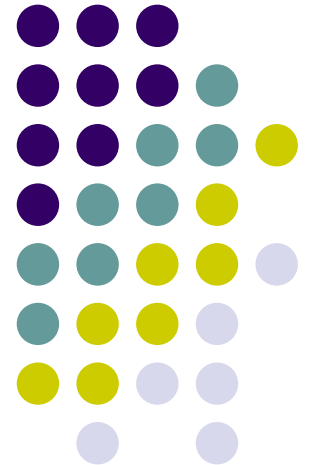


Laboratory Options for Computer Science Majors

Christopher Vickery

Tamara Blain

Queens College of CUNY



Outline



- Computer Science, Engineering, and Architecture
- Laboratory Models
- Software Options
- Hardware Platforms
- Conclusions

CS, CE, and CA

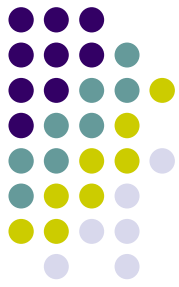


- The role of CS graduates in system design
 - Codesign can mean initial software description of entire system
 - Engineer wannabes or productive designers?
 - Is system design computer architecture?



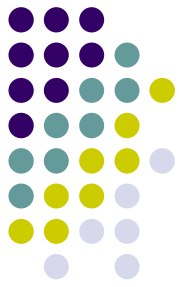
Laboratory Models

- Possible Goals
 - CPU Design
 - Paper machines, Subsets, IP cores
 - “Hardware Appreciation”
 - System Design
 - Architectures, Platforms, Systems, Circuits
- Simulation vs. Hardware Implementation
 - Hear, See, Do aphorism



Software Options

- Use C/C++/Java for simulation projects
- Use HDLs and simulation tools from vendors
 - Verilog and/or VHDL?
- Embedded systems software
 - Esterel ...
- System Implementation Languages
 - SystemC, SuperLog, Handel-C



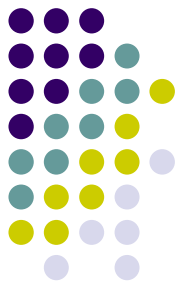
Hardware Platforms

- Circuit Breadboards
- FPGA Product Prototyping Boards
 - No peripherals, yet very expensive
- Student Laboratory Kits
 - Suitable for Logic Design
 - Suitable for System Design



Conclusions

- CS Students need to understand architecture, as always
- CS Students will be candidates for system design tasks previously in the CE-only realm
- Laboratory kits and development systems are available with very rich hardware feature sets accessible to people with software skills
- Our new environment: Handel-C and RC200
 - (Short demo)



Additional References

- Baily, Stephen. Comparison of VHDL, Verilog and SystemVerilog. www.model.com
- Gray, J. Hands-on Computer Architecture – Teaching Processor and Integrated Systems Design with FPGAs. WCAE 2000.
- Smith, D. J. VHDL & Verilog Compared & Contrasted Plus Modeled Example Written in VHDL, Verilog and C.
www.angelfire.com/in/rajesh52/verilogvhdl.html