NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS: Answer all short answer questions on your answer sheet. If no answer seems perfectly correct, select the best choice. Draw diagrams on the back of the question sheets.

BE SURE YOUR NAME IS PERFECT STUDENT AND THAT THE EXAM ID ABOVE MATCHES THE ONE ON YOUR ANSWER SHEET!

1. (5 Points) Which of the following is always necessary in order for a transition to take place in a finite state machine (FSM)?
   A. At least one input must be true.
   B. At least one input must be false.
   C. At least one output must be true.
   D. At least one output must be false.
   E. There must be a clock pulse.

2. (5 Points) Which of the following statements is true about a state diagram?
   A. The number of arcs going into each circle must be the same.
   B. The number of arcs leaving each circle must be the same.
   C. The arcs going into each circle must include all possible combinations of inputs.
   D. The arcs leaving each circle must include all possible combinations of inputs.
   E. The number of arcs leaving each circle must equal the number of arcs entering each circle.

3. (5 Points) Which of the following are inputs to the control unit of the CPU?
   A. The memory, the registers, and the disk.
   B. The opcode of the instruction.
   C. The ALU function code
   D. The cache, pipeline, and *rs* field.
   E. The control bits of the multiplexors.

4. (5 Points) Which of the following are outputs of the control unit of the CPU?
   A. The *rs*, *rt*, and *rd* fields of the instruction.
   B. The *Address* field of the instruction.
   C. The *opcode* field of the instruction.
   D. All of the above.
   E. None of the above.

5. (5 Points) Which of the following describes the *instruction fetch* operation?
   A. Memory[PC] <= IR
   B. IR <= Memory[PC]
   C. Memory[IR] <= PC
   D. PC <= Memory[IR]
   E. IR <= PC

6. (5 Points) Which of the following expressions represents the *effective address* of a *lw* or *sw* instruction?
   A. SignExtend(Instruction[0:15]) + Register[Instruction[21:25]]
   B. SignExtend(Instruction[21:25] + Register[Instruction[0:15]]
   C. SignExtend(Instruction[0:15] – Register[Instruction[21:25]]
   D. SignExtend(Instruction[21:25] – Register[Instruction[0:15]]
   E. PC + 4 * SignExtend(Instruction[0:15]

7. (5 Points) What are the possible input sources for the PC?
   A. The ALU, the Registers, and Data Memory
   B. The ALU, the Registers, and Instruction Memory
   C. (PC + 4), (SignExtend(Instruction[0:15]) * 4 + (PC + 4)), and ((PC+4)[28:31] | Instruction[0:25]*4)
   D. Instruction[0:15] + Register[Instruction[25:31], and ALU[3:7]
   E. SignExtend(Register[0]), and ALU[3:7]

8. (5 Points) Assume registers 0, 5, 6, and 7 contain the values 0x00000000, 0x00005555, 0x00006666, and 0x00007777 respectively. What register will change to what value as a result of executing the following instruction: *add $5, $6, $7*
   A. Register 0 will change to 0xFFFFFFFF
   B. Register 0 will change to 0x55556666
   C. Register 5 will change to 0x66667777
   D. Register 5 will change to 0x0000DDDD
   E. Register 6 will change to 0xCCCCCCCC

9. (5 Points) Assume the same initial register values as in Question 8. What register will change to what value as a result of executing *lui $5, 0x4004*
   A. Register 0 will change to 0x00004004
   B. Register 5 will change to 0x00004004
   C. Register 4 will change to 0x50004004
   D. Register 4004 will change to 0x00000005
   E. Register 5 will change to 0x40040000

10. (5 Points) Assume the same initial register values as in Question 8. What register will change to what value as a result of executing *and $0, $6, $7*
   A. No register will change
   B. Register 0 will change to 0x00007777
   C. Register 0 will change to 0x00006666
   D. Register 0 will change to 0x0000DDDD
   E. Register 0 will change to 0x11111111

11. (5 Points) Which statement describes the operation of the single cycle CPU implementation?
   A. The average number of clock cycles per instruction depends on the mix of instruction types executed.
   B. All instructions take the same amount of time to execute.
   C. Load instructions take longer to execute than any of the others.
   D. R-Type instructions execute faster than the others.
   E. Branch instructions execute faster than the others.

12. (5 Points) Which of the following describes the execution of R-type instructions?
   A. Read two registers, perform an ALU operation, and write to a register.
   B. Read two registers, perform an ALU operation, and write to data memory.
   C. Read one register, compute the branch target address, and write to two registers.
   D. Read one register, perform an ALU operation, and write to two registers.
   E. Read two registers from data memory, perform an ALU operation, and write to instruction memory.

13. (5 Points) What happens if an assembly language programmer writes “lw $a0, alpha($t0) and alpha represents the address 0x00400050?
   A. The assembler will put the value 0x00400050 in bits 0:15 of the instruction.
   B. The assembler will give an error because the value 0x00400050 won’t fit in bits 0:15 of the instruction.
   C. The assembler will give an error because the value 0x00400050 is not a word address.
   D. The assembler will put the value 0x400050 in bits 0:25 of the instruction.
   E. The assembler will substitute a sequence of *lui*, *ori*, and *lw* instructions for the programmer’s instruction.

14. (5 Points) What does an *slt* instruction do when it is executed?
    A. It subtracts the register selected by the rt field of the instruction from the register selected by the rs field of the instruction, and sets the register selected by the rd field of the instruction to 0x00000001 if the result is negative. Otherwise it sets the register selected by the rd field to 0x00000000.
    B. It subtracts the rt field of the instruction from the rs field of the instruction and sets the rd field of the instruction to 0x00000001 if the result is negative. Otherwise it sets the rd field to 0x00000000.
    C. It branches if the rs field of the instruction is less than the rt field of the instruction. Otherwise, it gets the next instruction from PC+4.
    D. It performs an end-around carry if the result of comparing the registers is negative zero.
    E. It tests the condition code to see if there was overflow, and performs a *sign-loss-trap* operation if there was.

15. (5 Points) What does the instruction "beq $5, $0, -6" do?
    A. It loads register 5 with the value –6.
    B. It subtracts 6 from register 0 and puts the result in register 5.
    C. It subtracts 24 from the PC if register 5 contains 0.
    D. It branches to address 0xFFFFFFFA
    E. It puts the contents of register 0 into the PC if register 5 contains –6.

16. (5 Points) What does the SPIM simulator do when it executes a *syscall* instruction?
    A. It loads a program into memory.
    B. It simulates various operating system functions, like writing to the console or exiting the program, depending on the value in register $v0.
    C. It translates the assembly language program into Java.
    D. It translates a Java program into MIPS assembly language.
    E. It pushes the parameters onto the stack and executes the return address three times.

17. (5 Points) Which sequence of MIPS instructions could be used to add 1 to a word of memory?
    A. increment word, load storage, store wordage
    B. store word, add immediate, load word
    C. load word, add immediate, store word
    D. load register, store register, increment word
    E. add register, branch equal, compare integer

18. (5 Points) The multi-cycle MIPS control unit can be in any of 10 different states. How many state flip-flops are needed for this control unit? (To be unambiguous: assume the control unit does *not* use "one hot encoding.")
    A. 1
    B. 2
    C. 4
    D. 8
    E. 16

19. (5 Points) What would be the advantage of adding an instruction register to the single-clock design of the control unit?
    A. Fetching the next instruction could be done at the same time as the execution of the current instruction.
    B. The instruction memory could be eliminated from the design.
    C. The ALU would have fewer propagation delays.
    D. Different instructions would take different amounts of time to execute.
    E. The clock would go slower, which reduces drain on the battery.

20. (5 Points) Draw a diagram that shows the inputs and outputs of the MIPS registers. Be sure to indicate how many bits each line represents. *Hint:* The "Read register 1" input has 5 bits.

21. (5 Points) Draw a state table for a modulo 4 counter that only increments when input X is true and which makes the output Z true only when the counter holds the binary representation of zero.