Course Outline

1. Measurement
    - 1.1. Units of Measure
        - 1.1.1. Orders of Magnitude
        - 1.1.2. Time (period, frequency)
        - 1.1.3. Information
        - 1.1.4. Rates (speed, bandwidth)
        - 1.1.5. Weighted Averages (CPI)
        - 1.1.6. Performance (Execution Time)
            - 1.1.6.1. Comparisons (ratios, percentages)
2. Logic Design
    - 2.1. Combinational Logic
        - 2.1.1. Truth Tables
        - 2.1.2. Boolean Functions
        - 2.1.3. Logic Networks
            - 2.1.3.1.Propagation Delays
        - 2.1.4. Karnaugh Map Minimization
    - 2.2. Combinational Building Blocks
        - 2.2.1. Decoders
        - 2.2.2. Multiplexers
        - 2.2.3. Adders
    - 2.3. ALU Design
        - 2.3.1. Two's Complement Arithmetic
        - 2.3.2. Parallel Adder
        - 2.3.3. MIPS ALU
    - 2.4. Sequential Logic
        - 2.4.1. Finite State Automata
            - 2.4.1.1. State Diagram
            - 2.4.1.2. State Table
            - 2.4.1.3. Combinational Logic and Storage Elements
                - 2.4.1.3.1. Moore Design
                - 2.4.1.3.2. Mealy Design
        - 2.4.2. Clocking
        - 2.4.3. Storage Elements
            - 2.4.3.1. R-S Latch
            - 2.4.3.2. Clocked R-S Latch
            - 2.4.3.3. Clocked D Latch
            - 2.4.3.4. D Flip-flop
                - 2.4.3.4.1. Master-Slave
                - 2.4.3.4.2. Edge Triggered
    - 2.5. Register File Design
3. Instruction Set Architectures
    - 3.1. RISC *vs* CISC
    - 3.2. MIPS
    - 3.3. Verilog Characterization

4. Datapath Design
    - 4.1. Single-cycle Design
    - 4.2. Pipelined Design
        - 4.2.1. Pipeline Principles and Terminology
            - 4.2.1.1. Bubbles, stalls, and delay slots
        - 4.2.2. Performance Measurement
        - 4.2.3. Structural, Control, and Data Hazards
        - 4.2.4. Register Forwarding and Branch Prediction
    - 4.3. Parallelism
        - 4.3.1. SIMD
        - 4.3.2. MIMD (Multicore)
        - 4.3.3. (GP)GPU; Nvidia, Larrabee
5. The Memory Hierarchy
    - 5.1. Principles: Cost, Capacity, Latency
    - 5.2. Levels: Cache, Primary Memory, Secondary
    - 5.3. SRAM Implementation
    - 5.4. DRAM Implementation
    - 5.5. Cache Design
        - 5.5.1. Direct Mapped, Set Associative
        - 5.5.2. Implementation
        - 5.5.3. Performance
6. Storage and I/O
    - 6.1. Disk Drives
        - 6.1.1. Structure
        - 6.1.2. Latency and Throughput
    - 6.2. Bus Hierarchies and Controllers