NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS:

- **Be sure your answer sheet has your name, not someone else's, pre-printed on it.**
- **Answer short answer questions on your answer sheet *in pencil.***
- **For True/False questions, mark "A" for True and "B" for False.**
- **It's okay to write on your exam sheets and/or to unstaple them, but don't put any stray marks on your answer sheet, and don't let it get folded.**
- **You are *not* allowed to use a calculator on this exam.**

1. If your name is A. Student, mark answer "A" for this question. If your name is not A. Student, get the exam and answer sheet with your name on it from Dr. Vickery now.

2. You have read and understand both the policy on cheating and the instructions written at the beginning of this exam. (True/False)

3. (4 Points) Which of the following best describes the components that would be used to construct R_0 of the ARC datapath?
   A. One D flip-flop and two tristate buffers.
   B. Thirty-two D flip-flops one AND gate, and 64 tristate buffers.
   C. Sixty-four tristate buffers.
   D. A wire.
   E. Six inverters, 64 AND gates, and an OR gate.

4. (4 Points) Which of the following best describes the components that would be used to construct A-Bus$_j$ of the ARC datapath?
   A. One D flip-flop and two tristate buffers.
   B. Thirty-two D flip-flops, one AND gate, and 64 tristate buffers.
   C. Sixty-four tristate buffers.
   D. A wire.
   E. Six inverters, 64 AND gates, and an OR gate.

5. (4 Points) Which of the following best describes the components that would be used to construct R_{ij} of the ARC datapath?
   A. One D flip-flop and two tristate buffers.
   B. Thirty-two D flip-flops, one AND gate, and 64 tristate buffers.
   C. Sixty-four tristate buffers.
   D. A wire.
   E. Six inverters, 64 AND gates, and an OR gate.

6. (4 Points) Which of the following best describes the components that would be used to construct R_i of the ARC datapath?
   A. One D flip-flop and two tristate buffers.
   B. Thirty-two D flip-flops, one AND gate, and 64 tristate buffers.
   C. Sixty-four tristate buffers.
   D. A wire.
   E. Six inverters, 64 AND gates, and an OR gate.

7. (4 Points) What states the purpose of a *sethi* instruction best?
   A. It can compare two values, and set the condition code bits to show the result.
   B. It can store a 32-bit two's complement number in memory.
   C. It can zero out the leftmost 22 bits of a microinstruction while leaving the other 19 bits unchanged.
   D. It can add a signed number to the PC.
   E. It can be used to put a number that can't be represented in 13 bits into a register.

8. (4 Points) What states the purpose of a *branch* instruction best?
   A. It can compare two values, and set the condition code bits to show the result.
   B. It can store a 32-bit two's complement number in memory.
   C. It can zero out the leftmost 22 bits of a microinstruction while leaving the other 19 bits unchanged.
   D. It can add a signed number to the PC.
   E. It can be used to put a number that can't be represented in 13 bits into a register.

9. (4 Points) Which of the following is the best definition of overflow?
   A. When the correct result of a calculation cannot be represented in the number of bits available.
   B. When you add two numbers and get a negative result.
   C. When you add two numbers and the carry out of the leftmost position is 1.
   D. When you add two numbers and the carry into the leftmost position is 0.
   E. When the answer is -2^{n-1} (n is the number of bits in the operands).

10. (4 Points) What will be the values of the C, V, N, and Z bits (in that order) after executing an ADDCC instruction with the values 0x00000000 and 0xFFFFFFFF on the A and B busses respectively? (*Remember: The N and Z bits are set according to the answer actually generated by the ALU, not according to what the answer "should" be.)*
   A. 0000
   B. 1001
   C. 0010
   D. 1010
   E. 1100

11. (4 Points) What will be the values of the C, V, N, and Z bits (in that order) after executing an ADDCC instruction with the values 0xFFFFFFFC and 0xFFFFFFFF on the A and B busses respectively? (*Remember: The N and Z bits are set according to the answer actually generated by the ALU, not according to what the answer "should" be.)*
   A. 0000
   B. 1001
   C. 0010
   D. 1010
   E. 1100

12. (4 Points) What will be the values of the C, V, N, and Z bits (in that order) after executing an ADDCC instruction with the values 0x80000000 and 0xFFFFFFFF on the A and B busses respectively? (*Remember: The N and Z bits are set according to the answer actually generated by the ALU, not according to what the answer "should" be.)*
   A. 0000
   B. 1001
   C. 0010
   D. 1010
   E. 1100

13. (4 Points) What will be the values of the C, V, N, and Z bits (in that order) after executing an ADDCC instruction with the values 0x00000001 and 0xFFFFFFFF on the A and B busses respectively? (*Remember: The N and Z bits are set according to the answer actually generated by the ALU, not according to what the answer "should" be.)*
   A. 0000
   B. 1001
   C. 0010
   D. 1010
   E. 1100

14. (4 Points) Convert the ARC ISA instruction 0x8E894006 to assembly language.
    A. andcc %r5, %r6, %r7
    B. andcc %r5, 6, %r7
    C. orncc %r5, %r6, %r7
    D. orncc %r5, 6, %r7
    E. addcc 5, 6, %r7

15. (4 Points) Convert the ARC ISA instruction 0x8E896006 to assembly language.
    A. andcc %r5, %r6, %r7
    B. andcc %r5, 6, %r7
    C. orncc %r5, %r6, %r7
    D. orncc %r5, 6, %r7
    E. addcc 5, 6, %r7

16. (4 Points) Assume registers 11, 9, and 10 contain the decimal values -1, 128, and 2 respectively. What register will change to what value as a result of executing *R[r11]* ← *srl(R[r9], R[r10])*?
    A. Register 11 will exchange values with register 2.
    B. Register 11 will change to 32
    C. Register 11 will change to 16
    D. Register 11 will change to 8
    E. Register 11 will change to 4

17. (4 Points) Translate the microinstruction in Question 16 into binary.
    A. 001001 0 001010 0 001011 0 00 0100 000 00000000000
    B. 001010 0 001011 0 001100 0 00 0100 000 00000000000
    C. 001011 0 001100 0 001101 0 00 0100 000 00000000000
    D. 001100 0 001101 0 001110 0 00 0100 000 00000000000
    E. 001101 1 001110 0 001111 0 00 0100 000 00000000000

18. (4 Points) How many clock cycles would it take to execute the microinstruction in Question 16?
    A. 1
    B. 2
    C. 3
    D. 4
    E. 5

19. (4 Points) How may states would it take to perform the same function as the microinstruction in Question 16 if the control unit was implemented using a Finite State Machine instead of a microprogram?
    A. 1
    B. 2
    C. 3
    D. 4
    E. 5

20. (4 Points) How many C Decoders are there in the ARC central processing unit?
    A. 1
    B. 2
    C. 3
    D. 4
    E. 5

21. (4 Points) How many A Multiplexors are there in the ARC central processing unit?
    A. 1
    B. 2
    C. 3
    D. 4
    E. 5

22. (4 Points) How many C Bus Multiplexors are there in the ARC central processing unit?
    A. 1
    B. 2
    C. 3
    D. 4
    E. 5

23. (4 Points) Which of the following is closest to the structure of an A Decoder in an ARC control unit?
    A. Six inputs and 64 outputs, but only 37 of the outputs are actually used.
    B. Six inputs and 64 outputs, but only 38 of the outputs are actually used.
    C. Twelve inputs and six outputs.
    D. Six inputs and twelve outputs, but only eight of the outputs are actually used.
    E. Six inputs and twelve outputs; all of the outputs are used.

24. (4 Points) How many tristate buffers does each output of an A Decoder go to?
    A. 32
    B. 37
    C. 38
    D. 64
    E. 32*37 (1,184)

25. (4 Points) Which of the following is closest to the structure of an A Multiplexor in the ARC central processing unit?
    A. Six inputs and 64 outputs, but only 37 of the outputs are actually used.
    B. Six inputs and 64 outputs, but only 38 of the outputs are actually used.
    C. Twelve inputs and six outputs.
    D. Six inputs and twelve outputs, but only eight of the outputs are actually used.
    E. Six inputs and twelve outputs; all of the outputs are used.

26. (4 Points) How many AND gates does the Clock go to in the register file?
    A. 32
    B. 37
    C. 38
    D. 64
    E. 32*37 (1,184)

27. (4 Points) How are the A, B, and C busses and the ALU used during a memory read operation?
    A. They are all disabled during memory write operations.
    B. The A Bus supplies the address, the B Bus supplies the Data, the ALU does anything that doesn't change the condition code flip-flops, and the C Bus gets sent to register 0.
    C. The A bus supplies the address, the B Bus may be connected to any register, the ALU does anything that doesn't change the condition code flip-flops, and the C Bus receives the data from memory.
    D. The A Bus receives the data, the B Bus receives the address, and the ALU receives the read function code. The C Bus is tristated.
    E. The A and B busses send and receive the data, the C Bus sends the address, and the ALU is not used.

28. (4 Points) What are the addresses of the first three microinstructions that will execute to fetch and execute an andcc ISA instruction?
    A. 0, 1, 2
    B. 0, 1, 1604
    C. 0, 1, 1608
    D. 0, 1, 1688
    E. 0, 1, 1760