NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS: Be sure your answer sheet has *your* name on it. Answer all questions on your answer sheet using a No. 2 pencil. Be sure not to make any stray marks on your answer sheet, and don't bend or fold it. Select the best answer for each question from the choices given. For True/False questions, select A for True or B for False.

You may *not* use a calculator for this exam.

1. (3 Points) I have read the above Instructions for this exam. (True/False) *Hint: The instructions tell how to answer questions like this.*

2. (3 Points) What is the main reason for having a hierarchy of memories in a computer system?
   A. Because L1 cache is non-volatile.
   B. Because main memory has a shorter access time than the registers.
   C. Because disks are volatile.
   D. Because disks are not part of the storage hierarchy.
   E. Because it would be prohibitively expensive to make a single memory system with the capacity of a disk and the access time of the registers.

3. (3 Points) Which of the following is the best describes a *RAM IC*?
   A. One bit of memory.
   B. Has a Chip Select input.
   C. Has separate memories for instructions and data.
   D. Is constructed from multiple chips.
   E. Uses electroluminescent photonic emission sensors to control color temperatures of the matrices.

4. (3 Points) Which of the following best describes a *binary cell*? Use the same choices as Question 3.

5. (3 Points) Which of the following best describes a *split cache*? Use the same choices as Question 3.

6. (3 Points) Which of the following best describes a *memory system*? Use the same choices as Question 3.

Questions 7 through 14 are based on a 4096 x 8 memory system constructed from 1024 x 4 RAM ICs.

7. (3 Points) How many *rows* of RAM ICs would there be in this memory system?
   A. 2
   B. 4
   C. 8
   D. 16
   E. 32

8. (3 Points) How many *columns* of RAM ICs would there be in this memory system?
   A. 2
   B. 4
   C. 8
   D. 16
   E. 32

9. (3 Points) How many bits are there in the memory system?
   A. 8K
   B. 12K
   C. 16K
   D. 24K
   E. 32K

10. (3 Points) How many address wires go into the memory system?
    A. 10
    B. 11
    C. 12
    D. 13
    E. 14

11. (3 Points) How many address wires go into each RAM IC?
    A. 6
    B. 8
    C. 10
    D. 11
    E. 12

12. (3 Points) What are the dimensions of the decoder used by the memory system to select a row of RAM ICs?
    A. 1 x 2
    B. 2 x 4
    C. 3 x 8
    D. 4 x 16
    E. 5 x 32

13. (3 Points) What are the dimensions of the decoder inside each RAM IC for selecting a row of binary cells?
    A. 6 x 64
    B. 8 x 256
    C. 10 x 1024
    D. 11 x 2048
    E. 12 x 4096

14. (3 Points) How many binary cells are there in each RAM IC?
    A. 512
    B. 1536
    C. 2048
    D. 4096
    E. 8192

15. (3 Points) Which of the following is *not* a Programmable Logic Device?
    A. ROM
    B. PROM
    C. PLA
    D. PAL
    E. FPGA

16. (3 Points) Which of the following consists of a decoder connected to a programmable fuse matrix? Use the same choices as Question 15.

17. (3 Points) How many OR gates would a 32 x 8 PROM have?
    A. 4
    B. 8
    C. 12
    D. 16
    E. 32

18. (3 Points) How many AND gates would a 32 x 8 PROM have?
    A. 4
    B. 8
    C. 12
    D. 16
    E. 32

19. (3 Points) How many fuses would a 32 x 8 PROM have?
    A. 2^{28}
    B. 128
    C. 256
    D. 384
    E. 512

20. (3 Points) Which of the following best describes a *cache miss?*
    A. A mechanism for associating memory addresses with disk sectors.
    B. A memory inside the cache that contains housekeeping information.
    C. A request for a word of memory from a direct mapped cache.
    D. A request for a word of memory that is not in the cache.
    E. A block of main memory that has been copied into cache.

21. (3 Points) A computer has a main memory with an access time of 850 nsec and a single cache with an access time of 60 nsec. A program runs on this computer with a hit ratio of 0.90. What is the average access time for this program?
    A. 137 nsec
    B. 138 nsec
    C. 139 nsec
    D. 140 nsec
    E. 141 nsec

22. (3 Points) Which of the following terms describes a *fully associative* cache system?
    A. Read operations go through the cache, but not write operations.
    B. Write operations go through the cache, but not read operations.
    C. A main memory block might be loaded into any cache slot.
    D. Each main memory block is always loaded into a single cache slot.
    E. Each cache slot is associated with a single main memory block.

23. (3 Points) Which of the following terms describes a *direct mapped* cache system? Use the same choices as Question 22.

24. (3 Points) If memory accesses were completely random, the hit ratio for a program would be expected to equal:
    A. The size of the cache divided by the size of main memory.
    B. The size of main memory divided by the size of the cache.
    C. The access time of the cache divided by the access time of main memory.
    D. The access time of main memory divided by the access time of the cache.
    E. The size of a memory block divided by the size of a cache line.

25. (3 Points) Why are hit ratios so much higher than what would be expected given random accesses?
    A. Cache memory accesses are much faster than main memory accesses.
    B. Cache memory is directly mapped but main memory is associative.
    C. The cache reads more than just the single location requested by the CPU, and the locality principle makes these extra locations very likely to be requested by the CPU in the future.
    D. The cache always picks a random line for replacement, which offsets the random accesses the CPU requests.
    E. Actually, cache hit ratios are lower than what would be expected, not higher.

Questions 26 through 28 are based on a cache system with 2^{26} bytes of main memory, 16 bytes per cache slot, and 2^{10} cache slots.

26. (3 Points) How many bits wide would the tag field be for a fully associative cache?
    A. 18
    B. 20
    C. 22
    D. 24
    E. 26
27. (3 Points) How many bits wide would the tag field be for a direct mapped cache?
    A. 15
    B. 14
    C. 13
    D. 12
    E. 11
28. (3 Points) How many sets would there be for a set associative cache with a set size of 8?
    A. 64
    B. 128
    C. 256
    D. 512
    E. 1024
29. (3 Points) What is the bandwidth of a bus with 32 data wires and a clock speed of 128 MHz? Give the numerical value here. The next question asks for the unit of measure.
    A. 1.024
    B. 2.048
    C. 4.096
    D. 8.192
    E. 16.384
30. (3 Points) What is the unit of measure for the answer to the previous question?
    A. MHz
    B. GHz
    C. Mbps
    D. Gbps
    E. KB
31. (3 Points) A UART is an example of a:
    A. Library Function
    B. File Driver
    C. Device Driver
    D. Interrupt Service Routine
    E. Device Controller
32. (3 Points) What is a bus bridge?
    A. A device that links the L1 cache to the L2 cache.
    B. A device that compensates for the difference in bandwidths of two busses.
    C. A device that connects the address wires to the data wires in a bus.
    D. A device that connects the address wires to the control wires in a bus.
    E. A device that connects the control wires to the data wires in a bus.
33. (3 Points) What is the role of the Receive Buffer Register in a UART?
    A. It holds data that the CPU has written to the bus but which has not yet reached the UART.
    B. It holds interrupt requests.
    C. It holds data that is ready for the CPU to read.
    D. It contains the address of an interrupt service routine.
    E. It synchronizes the IIE and the IIR registers.
34. (3 Points) What is (are) the advantage(s) of a Direct Memory Access system?
    A. It reduces the bandwidth of the data bus.
    B. It increases the bandwidth of the control bus.
    C. It can reduce the number of interrupts needed to complete a data transfer.
    D. It can reduce the number of bus cycles needed to complete a data transfer.
    E. Both C and D.