NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS: Answer all questions in your examination book *in sequence*. Legibility counts!

1. Did you read the Instructions, located approximately 3/8" above the words you are reading now?
2. Write your name and exam ID () on the front cover of your exam booklet.
3. Define the term *Instruction Set Architecture*, and answer each of the following questions about ISA styles:
   A. Tell what the acronyms *RISC* and *CISC* stand for.
   B. Describe two characteristics that differentiate between these two ISA styles.
   C. Name one commercial processor (or processor family) that is a member of each style.
   D. Which style does the ARC processor used in the book use?
4. Draw bit *j* of Register *i* of the ARC processor. Show the multiplexer(s), decoder(s), and gate(s) that would be used to connect this bit to the three busses and the system clock. Indicate what parts of the IR would control the multiplexers and decoders to the extent that we have covered that topic in class.
5. What operations must be performed by the CPU during the fetch part of the fetch-execute cycle? Name the specific registers involved and use sentences to tell what role each register plays.
6. Draw the leftmost and rightmost bits of an adder/subtractor, including the logic to generate the values of the condition code bits. You don't have to draw the gates inside the full adders, but you have to show the gates that allow the circuit to either add or subtract depending on the value of an input signal named "*subtract.*" When *subtract* is one, the device performs two's complement subtraction, and when *subtract* is zero, the device performs two's complement addition. Label all inputs and outputs meaningfully.
7. Assume there is a two's complement adder/subtracter that works with 4-bit operands. Answer the following questions about the operation of this device:
   A. What is the range of two's complement numbers that can be represented in 4 bits?
   B. What will be the values of the 4 condition code bits if the decimal values +2 and –5 are added together?
   C. What will be the values of the 4 condition code bits if the decimal values +5 and + 6 are added together. (*Hint:* Your answer to part A should have an upper limit less than +11.) *Bonus:* What will be the decimal value the device will produce as the "answer"?
8. Write sentences that tell the result of executing each of the following ARC instructions:
   A. ld %r5, %r6, %r7
   B. ld %r5, 6, %r7
   C. addcc %r5, %r6, %r7
   D. addcc %r5, 6, %r7
9. Translate the following instruction into binary. The leftmost two bits of arithmetic instructions are binary 10, and the op3 field of *orcc* instructions is binary 010010. You can get partial credit for this question if you include a diagram that shows the various fields of the instruction and how the assembly language relates to those fields, even if you don't get the layout exactly right.

   orcc %r1, -5, %r0

10. Give a step-by-step description of what the ARC CPU does to execute the instruction in Question 9.