NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS: Be sure your answer sheet has *your* name, student ID, and exam ID printed on it. Pick the *best* answer for each question.

1. Which of the following best describes the ARC ALU's *simm13* function:

   A. Result is bits 0:12 of the A operand, sign extended.
   B. Result is bits 0:12 of the A operand padded left with zeros.
   C. Add 4 to the A operand.
   D. Add 1 to the A operand.
   E. Add A operand and B operand; update condition codes.

2. Which of the following best describes the ARC ALU's *addcc* function:
   A. Result is bits 0:12 of the A operand, sign extended.
   B. Result is bits 0:12 of the A operand padded left with zeros.
   C. Add 4 to the A operand.
   D. Add 1 to the A operand.
   E. Add A operand and B operand; update condition codes.

3. Which of the following best describes the ARC ALU's *incpc* function:
   A. Result is bits 0:12 of the A operand, sign extended.
   B. Result is bits 0:12 of the A operand padded left with zeros.
   C. Add 4 to the A operand.
   D. Add 1 to the A operand.
   E. Add A operand and B operand; update condition codes.

4. Which of the following best describes the ARC ALU's *sext13* function:
   A. Result is bits 0:12 of the A operand, sign extended.
   B. Result is bits 0:12 of the A operand padded left with zeros.
   C. Add 4 to the A operand.
   D. Add 1 to the A operand.
   E. Add A operand and B operand; update condition codes.

5. What rule best describes how the V condition code bit's value is determined:
   A. It is set to 1 if C is 0, and it is set to 0 if C is 1.
   B. It is set to 0 if C is 0 and it is set to 1 if C is 1.
   C. It is set to 1 if two positive numbers are added and the result is negative or if two negative numbers are added and the result is positive. Otherwise, it is set to 0.
   D. It is set to 1 if the carry out of the leftmost bit is 1 and the sign of the result is 1. Otherwise it is set to 0.
   E. It is set to 0 if the carry out of the leftmost bit is 0 and the sign of the result is 0. Otherwise it is set to 1.

6. What is the purpose of the A-Mux, B-Mux, and C-Mux bits in ARC microinstructions?
   A. To control whether the register numbers come from the rs_1, rs_2, and rd fields of the IR or from the A, B, and C fields of the microinstruction.
   B. To select which answer the ALU is to output after it has calculated all possible answers.
   C. To allow information to be shared across busses.
   D. To indicate whether the busses connect to memory or to the ALU.
   E. To override the special meaning of register 0.

Questions 7 through 12 refer to the following sample output from the ARC simulator that "we" wrote this semester. Line numbers (1-30) have been added so they can be referenced in the questions.

```
 1 Processing file: exam.bin
 2 Memory initialized. 1048576 bytes available.
 3 Program loaded.  First non-zero location is 00012C
 4     Register  32 changes to  0000012C
 5 First instruction found at 00012C
 6     Memory at 00012C returns D6002190
 7     Register  37 changes to  D6002190
 8              PC: 00012C  IR: D6002190  ld
 9     Register  33 changes to  00000190
10     Memory at 000190 returns 00000007
11     Register  11 changes to  00000007
12     Register  32 changes to  00000130
13     Memory at 000130 returns 9802E005
14     Register  37 changes to  9802E005
15              PC: 000130  IR: 9802E005  add
16     Register  12 changes to  0000000C
17     Register  32 changes to  00000134
18     Memory at 000134 returns 8083000C
19     Register  37 changes to  8083000C
20              PC: 000134  IR: 8083000C  addcc
21     Register  00 changes to  00000000
22     Register  32 changes to  00000138
23     Memory at 000138 returns 9533000B
24     Register  37 changes to  9533000B
25              PC: 000138  IR: 9533000B  srl
26     Register  10 changes to  00000000
27     Register  32 changes to  0000013C
28     Memory at 00013C returns 91D02000
29     Register  37 changes to  91D02000
30              PC: 00013C  IR: 91D02000  halt
```

7. Why does register 32 change to 12C at the beginning?
   A. Because 12C is the op code for the *ld* instruction.
   B. Because register 32 holds the instruction being executed.
   C. Because the pc has to get the address of the first instruction to execute.
   D. Because the Decode operation for an *ld* instruction has the value 300.
   E. Because the Decode operation for an *ld* instruction has the value 32.

8. The lines, such as 6 and 13, that say "Memory at xxx returns yyy" reflect what operation?
   A. Connecting a register to the ALU.
   B. Reading from memory address xxx.
   C. Writing to memory address xxx.
   D. Reading from memory address yyy.
   E. Writing to memory addrss yyy.

9. What best describes the situation on line 7?
   A. An instruction has been read from memory and is being placed in the ir.
   B. The pc is being updated to prepare for fetching the next instruction.
   C. A *srl* instruction has computed a value, which is being discarded.
   D. A *srl* instruction has computed a value, and it is being saved in general register 37.
   E. The contents of register 37 are being added to the contents of register 32.

10. Translate the contents of the ir on line 20 to assembly language.
   A. addcc %r1, %r2, %r3
   B. ld 0x190, %r11
   C. add %r11, 5, %r12
   D. addcc %r12, %r12, %r0
   E. srl %r12, %r11, %r10

11. How many clock cycles were there from line 6 through line 30?
    A. 4
    B. 5
    C. 14
    D. 20
    E. 25

12. What is register 33 being used for in line 9?
    A. To set up the results of the *add* instruction on line 15.
    B. For computing the effective address of the *ld* instruction on line 8.
    C. To hold the address of the next instruction to execute.
    D. To hold the instruction being executed.
    E. To receive the results of unwanted calculations.

13. In a microprogrammed implementation of the ARC CPU, there are ___ clock cycles per microinstruction.
    A. 0
    B. 1
    C. 2
    D. It depends on the ISA instruction being executed.
    E. It depends on the ALU function code.

14. What best describes the purpose of the *decode* operation of a microinstruction (when the microinstruction COND field is 111_2).
    A. It translates an ISA instruction from assembly language to binary.
    B. It translates an ISA instruction from binary to assembly language.
    C. It translates an ISA instruction from RAM to ROM.
    D. It determines the address of the next microinstruction based on the ISA instruction.
    E. It converts octal numbers to binary.

15. Define *memory hierarchy*.
    A. The rate at which information can be transferred from one place to another.
    B. Ordering storage systems according to their speed, capacity, and cost.
    C. When the CPU tries to read from a memory location and it has to wait for the information to be retrieved from main memory.
    D. An I/O device, such as a keyboard, that is used to control a computer.
    E. A circuit that interfaces between a peripheral device and a bus connected to the CPU.

16. Define *device controller*.
    A. The rate at which information can be transferred from one place to another.
    B. Ordering storage systems according to their speed, capacity, and cost.
    C. When the CPU tries to read from a memory location and it has to wait for the information to be retrieved from main memory.
    D. An I/O device, such as a keyboard, that is used to control a computer.
    E. A circuit that interfaces between a peripheral device and a bus connected to the CPU.

17. Define *bandwidth*.
    A. The rate at which information can be transferred from one place to another.
    B. Ordering storage systems according to their speed, capacity, and cost.
    C. When the CPU tries to read from a memory location and it has to wait for the information to be retrieved from main memory.
    D. An I/O device, such as a keyboard, that is used to control a computer.
    E. A circuit that interfaces between a peripheral device and a bus connected to the CPU.

18. Define *cache miss*.
    A. The rate at which information can be transferred from one place to another.
    B. Ordering storage systems according to their speed, capacity, and cost.
    C. When the CPU tries to read from a memory location and it has to wait for the information to be retrieved from main memory.
    D. An I/O device, such as a keyboard, that is used to control a computer.
    E. A circuit that interfaces between a peripheral device and a bus connected to the CPU.

19. What are the two factors that determine the bandwidth of a communication channel?
    A. The frequency and the amplitude of the wave.
    B. The pitch and the timbre of the sound.
    C. The wavelength and the hue of the light.
    D. The number of flip-flops and the number of bus wires.
    E. The number of bits per transfer and the number of transfers per second.

20. An ARC program executes 1,000 instructions. 10% are *st* and 15% are *ld* instructions. What is the total number of memory access needed to process this program?
    A. 100
    B. 150
    C. 250
    D. 1000
    E. 1250

21. What are the RBR and the THR?
    A. Multiplexers that control the connections between busses and the ALU.
    B. Fields of a microinstruction for branching and doing calculations.
    C. Cache control bits used to determine which cache line to replace.
    D. The Rise Bounce Rate and Task Hit Rate of a clock signal.
    E. Data registers in a UART that the CPU can read and write.

22. What will be the average memory access time for a program with a cache hit ratio of 90% if there is one cache with an access time of 1 nsec and main memory has an access time of 10 nsec? Assume that when there is a cache miss the access time is only the main memory access time, not the main memory access time plus the cache access time.
    A. 320 nsec.
    B. 280 nsec.
    C. 235 nsec.
    D. 190 nsec.
    E. 145 nsec.