NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS: Choose the best choice for multiple choice questions. There is no penalty for guessing. Fill in the blank for fill in the blank questions. Answer on the backs of the exam sheets for questions that say to do so. Be sure to write the number of each such question next to your answer.
The number of points indicated for each question are relative values, not absolute.

Answer the following questions about the three CPU designs covered in the textbook: (Single-cycle, Multiple-cycle, and Pipelined). The single-cycle and multiple-cycle designs were covered in chapter 5, and the pipelined design was covered in chapter 6.

1. (5 Points.) Which choice best characterizes the *pipelined* design?
   A. The clock period has to be long enough to process the longest instruction.
   B. Different instructions use different numbers of clock cycles, depending on how many steps are needed to fetch and execute them.
   C. All instructions take the same number of clock cycles to fetch and execute, but a new instruction may complete execution as often as one per clock cycle.
   D. The number of instructions executed per clock cycle is an integer multiple of each instruction's operation code field.
   E. Each instruction requires 2^n clock cycles to process, where *n* is the number of stages.

2. (5 Points.) Which choice best characterizes the *single-cycle* design?
   A. The clock period has to be long enough to process the longest instruction.
   B. Different instructions use different numbers of clock cycles, depending on how many steps are needed to fetch and execute them.
   C. All instructions take the same number of clock cycles to fetch and execute, but a new instruction may complete execution as often as one per clock cycle.
   D. The number of instructions executed per clock cycle is an integer multiple of each instruction's operation code field.
   E. Each instruction requires 2^n clock cycles to process, where *n* is the number of stages.

3. (5 Points.) Which choice best characterizes the *multiple-cycle* design?
   A. The clock period has to be long enough to process the longest instruction.
   B. Different instructions use different numbers of clock cycles, depending on how many steps are needed to fetch and execute them.
   C. All instructions take the same number of clock cycles to fetch and execute, but a new instruction may complete execution as often as one per clock cycle.
   D. The number of instructions executed per clock cycle is an integer multiple of each instruction's operation code field.
   E. Each instruction requires 2^n clock cycles to process, where *n* is the number of stages.

4. (5 Points.) What would be the clock speed (frequency) of a perfectly balanced 5-stage pipelined implementation compared to a single-cycle implementation of some architecture?
   A. The same as the clock speed of the single-cycle implementation
   B. Five times faster than the clock speed of the single-cycle implementation
   C. One fifth as fast as the clock speed of the single cycle implementation
   D. Twenty per cent faster than the clock speed of the single cycle implementation
   E. Eighty percent as fast as the clock speed of the single cycle implementation

5. (5 Points.) What is a pipeline's *latency*?
   A. The delay between fetching and executing an instruction
   B. The delay from the end of executing one instruction and starting to fetch the next one
   C. The delay from the time an instruction enters the pipeline until it completes execution
   D. The delay from the beginning of one stage to the beginning of the next one
   E. The delay from the end of one stage to the beginning of the next one

6. (5 Points.) How many pipeline registers would a processor with a seven stage pipeline have?
   A. Four
   B. Five
   C. Six
   D. Seven
   E. Eight

7. (5 Points.) How many bits are there in ID/EX.rt? (*Hint: the answer to this question is different from the answer to the next one.*)
   _____ bits.

8. (5 Points.) How many bits are there in ID/EX.Register[rt]?
   _____ bits.

9. (5 Points.) A conflict in which a hardware unit is needed by more than one stage of a pipeline at the same time is called:
   A. A data hazard
   B. A computation hazard
   C. A control hazard
   D. A structural hazard
   E. A biohazard

10. (5 Points.) A conflict in which an instruction needs the result of another instruction that hasn't completed its execution yet is called:
    A. A data hazard
    B. A computation hazard
    C. A control hazard
    D. A structural hazard
    E. A biohazard

11. (5 Points.) A conflict in which one or more wrong instructions enter the pipeline because of a conditional branch instruction is called:
    A. A data hazard
    B. A computation hazard
    C. A control hazard
    D. A structural hazard
    E. A biohazard

12. (10 Points.) Describe in your own words what problem register forwarding solves and the mechanics of how it works. You may use a mix of diagrams and/or pseudocode, but the core of your answer must be well-formed English sentences. Answer on the back of one of the exam sheets.

13. (5 Points.) What is a *delay slot*?
    A. A place to keep delays
    B. A pipeline bubble
    C. A pipeline stall
    D. The instruction immediately after a branch instruction
    E. An extra clock cycle used to synchronize the CPU clock with main memory

14. (5 Points.) What are the parameters that vary with a component's position in the memory hierarchy?
    A. Speed, access time, and average propagation delay
    B. Effective address, physical address, and virtual address
    C. Cost per bit, access time, and capacity
    D. Cost per bit, block size, and width of the index field
    E. Pages per sector, sectors per track, and tracks per cylinder

15. (5 Points.) Where is the biggest difference in access times?
    A. Between the CPU and the cache
    B. Between the L1 and L2 caches
    C. Between the cache and main memory
    D. Between main memory and the disk
    E. Between RAM and ROM

16. (5 Points.) Explain your answer to the previous question on the back of an exam sheet.

The following questions relate to the design of a cache memory for a system with 2^{40} bytes of byte-addressable main memory, 2^{16} cache lines, 64 bytes per cache line, and a 4-way set-associative design.

17. (5 Points.) How many bits in a memory address? _____

18. (5 Points.) How many bits in the offset field of an address? _____

19. (5 Points.) How many bits in the index field of an address? _____

20. (5 Points.) How many bits in the tag field of an address? _____

21. (5 Points.) How many blocks are there in main memory? _____

22. (5 Points.) How many sets are there in the cache? _____

23. (5 Points.) What is the total number of bits in the cache? Show your work (in the margin) to be eligible for partial credit: _____

24. (5 Points.) What is the difference between *write through* and *write back*?
    A. Write through refers to disk storage and write back refers to cache storage.
    B. Write through refers to cache storage and write back refers to main memory storage.
    C. Write through copies information to main memory immediately, but write back delays writing to memory until it's necessary.
    D. Write through saves writes until the CPU is through with the data, and write back keeps a copy so the CPU can get it back.
    E. Write through uses cache snooping, but write back uses disk scheduling.

25. (5 Points.) Define *temporal locality* on the back of an exam sheet, and tell what it has to do with memory hierarchies.

26. (5 Points.) What is the average access time for a processor with a 100 psec access time to cache, a 1 nsec access time to main memory, and a hit ratio of 0.95? Give your answer in nanoseconds: _____ nsec.

27. (5 Points.) What is the purpose of a *page table*?
    A. It is used by the CPU to translate virtual page numbers to physical page numbers
    B. It is used by the operating system to keep track of the pages in a document
    C. It is used by the cache to translate cache lines to memory blocks
    D. It is used by the cache to tell whether a page has been written to or not
    E. It is used by the translation lookaside buffer to tell whether another cache has information needed by its own CPU

28. (5 Points.) What is a *translation lookaside buffer*?
    A. The bits in a cache that tell whether a line is valid and/or dirty
    B. A memory in the cache that tells what memory block occupies each line
    C. A cache in the CPU that holds parts of a page table
    D. Storage for the victim in a write back design
    E. A table that the operating system uses to keep track of memory blocks on disk

29. (5 Points.) The operating system updates the page table for a process when there is a page fault, and the CPU uses the page table to translate virtual addresses to physical addresses.
    A. True
    B. False

30. (5 Points.) A subroutine in the operating system detects page faults.
    A. True
    B. False