NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS: Answer the first and last questions on the exam sheets. Answer all other questions in your examination booklet, *in sequence, please.* All questions count equally, even the really short ones, like 4 and 9.

1. List the seven input/output connections of the MIPS register file. For each one, tell the name, how many bits wide it is, whether it is an input or an output, and what it is used for. I have completed the first one and part of the second one for you:

Name	Width	Input or Output	Use
RegWrite	1	Input	Controls whether a register will be written to or not.
Read register 1			

2. Draw a diagram that shows how all the inputs and outputs from Question 1 would connect to one bit (R_{ij}) of one register in the register file. In addition to the one flip-flop, you will need to show how the flip-flop connects to a decoder, two multiplexers, and an AND gate. You may use tristate buffers instead of the two multiplexers if you prefer. Use the subscript *i* when wires are associated with the register, and *j* when wires are associated with a particular bit position within the register.

3. Completely describe the processing of *lw* instructions in English sentences. (No Verilog, no diagrams.) Just give the algorithm that must be followed, not how it is actually implemented in either of the datapaths from Chapter 5. Look at Question 11 before you answer this question to be sure your answer here does not duplicate your answer there.

4. What is special about Register zero?

5. Translate this instruction into assembly language: 0x3C0FABCD. Assuming Register 15 contains 0x12345678 before this instruction is executed, what will it contain afterwards?

6. Memory location 0x00400028 contains 0x11EFFFFF. What will be the contents of the program counter after this instruction is executed? Show all work for partial credit.

7. How long would it take a program take to execute one million instructions, given the following parameters: 5 MHz clock speed. 40% of the instructions require one clock cycle to process, 40% require 2 clock cycles, and the rest require 3 clock cycles. Show all work for partial credit. Be sure to give the proper units of measure for all calculations.

8. In the single cycle datapath, there are two adders, one for incrementing the PC and one for computing the branch target address. Why can't these operations be done using the ALU?

9. How many gates and how many flip-flops are needed to sign extend a 16-bit value to 32 bits?

10. Both the single cycle datapath and the multi-cycle datapath have a multiplexer with inputs from either bits 16-20 or 11-15 of the instruction. The multiplexer is controlled by a signal named *RegDst*. Explain what purpose this multiplexer and its control bit serves.

11. List the sequence of states that the multi-cycle datapath would go through to fetch and execute an *lw* instruction. Tell what happens in each state.

12. Tell how *price*, *access time*, and, *storage capacity* are related across the levels of a *memory hierarchy*.

13. Name and describe the two types of *locality* that programs exhibit, and explain why they are important in the success of cache memory systems.

14. What is the average access time of a memory system with one level of cache if main memory access time is 1 nanosecond, cache access time is 200 picoseconds, and the hit ratio is 0.9? Be sure to indicate the unit of measure for your answer.

15. A byte-addressable memory has 2^{20} 24-bit words and a direct-mapped cache with 128 cache lines. Each cache line holds 16 words of memory. Give the values of the following items. For items F, G, and H, you don't have to do the arithmetic as long as you give the correct arithmetic expression.

    A. _____ Number of address bits

    B. _____ Number of tag bits

    C. _____ Number of index bits

    D. _____ Number of block offset bits

    E. _____ Number of byte offset bits

    F. _____ Number of data bits per cache line

    G. _____ Total number of bits per cache line

    H. _____ Total number of bits in the cache