NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS: Circle the letter of the best choice for each multiple choice question. For diagram questions, draw the diagram on the back of any exam sheet. <u>Be sure to write the question number next to each diagram.</u> Except where otherwise indicated, all questions count equally. USE PENCIL IF YOU HAVE ONE.

- 1. (4 Points) What is the preferred instrument to use for answering questions on this exam?
 - A. Pencil
 - B. Pen
 - C. Crayon
 - D. Paint
 - E. Charcoal
- 2. (4 Points) What type of gate will produce a value of *true* if its inputs are different from each other?
 - A. AND
 - B. OR
 - C. NAND
 - D. NOR
 - E. XOR
- 3. (4 Points) What single gate could be used to detect overflow during two's complement addition or subtraction?
 - A. AND
 - B. OR
 - C. NAND
 - D. NOR
 - E. XOR
- 4. (4 Points) What is the decimal value of the 16 bit two's complement number 0xFFFE?
 - A. 65,634
 - B. 0
 - C. -1
 - D. –2
 - E. +3
- 5. (4 Points) What is the smallest number of flip-flops that could be used to build a finite state machine that has a clock with a period of one day and that keeps track of the day of the week?
 - A. 0
 - B. 1
 - C. 3
 - D. 6
 - E. 7

6.

- (4 Points) In a finite state machine, the present state is given by which of the following:
 - A. The D outputs of the flip-flops
 - B. The Q outputs of the flip-flops
 - C. The D inputs of the flip-flops
 - D. The D outputs of the flip-flops
 - E. The clock inputs of the flip-flops
- 7. (4 Points) In a finite state machine, state transitions happen only:
 - A. When there is a clock pulse
 - B. When the present state is the same as the next state
 - C. When the present state is causes the next state to reset
 - D. When the reset causes a clock pulse on the D outputs of the flip-flops
 - E. When the latches cause the Q inputs of the flip-flops to toggle

Perfect Student	First Exam	3/6/2007	
Exam ID: 5211	CS-343/Vickery	Page 2 of 3	

- 8. (4 Points) In a finite state machine, the outputs of the combinational logic go to
 - A. The clock generator
 - B. The latch outputs
 - C. The condition code bits
 - D. The pushbuttons
 - E. The D inputs of the flip-flops
- 9. (4 Points) How many flip-flops are there in a 32-bit parallel adder?
 - A. 0
 - B. 32
 - C. 64
 - D. 96
 - E. 128
- 10. (4 Points) What limits the maximum rate at which the clock of a finite state machine can be operated?
 - A. The number of inputs to the combinational logic
 - B. The number of outputs from the combinational logic
 - C. The number of flip-flops
 - D. The propagation delays in the combinational logic
 - E. The number of latches in the combinational logic
- 11. (4 Points) Draw the Karnaugh Map for the following function and write the minimized equation:

a	b	с	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

- 12. (4 Points) A disk is rotating at 7200 RPM. How long does it take to make one complete revolution?
 - A. 8.3 seconds
 - B. 8.3 milliseconds
 - C. 83 milliseconds
 - D. 8.3 microseconds
 - E. 83 microseconds
- 13. (4 Points) What is the frequency of a clock with a period of 500 picoseconds?
 - A. 0.00000000500 seconds
 - B. 500 GHz
 - C. 2 GHz
 - D. 0.5 nanoseconds
 - E. 42
- 14. (4 Points) What bandwidth is required to transmit 30 network requests per second if each request is 64 KB (kilobytes) on average? (Pick the closest answer.)
 - A. 2 kilobytes per second
 - B. 16 kilobytes per second
 - C. 2 megabytes per second
 - D. 16 megabytes per second
 - E. 2 gigabytes per second

- 15. (4 Points) Which of the following is an on/off switch controlled by electricity?
 - A. Pushbutton
 - B. Slide switch
 - C. LED
 - D. Seven segment display
 - E. Transistor
- 16. (4 Points) Segments A, B, and C are on.
 - A. F
 - B. 5
 - C. 6
 - D. 9
 - E. 7
- 17. (4 Points) 0xD
 - A. 1101
 - B. 1011
 - C. 0101
 - D. 1100
 - E. 1110
- 18. (4 Points) What is the name of the logic circuit that would be used to control which of two signals would be passed to another part of a design? (The one we used for selecting the fast or slow clock signal in the calendar state machine, for example.)
 - A. Full adder
 - B. Half adder
 - C. Decoder
 - D. Multiplexer
 - E. Flip-flop
- 19. (4 Points) Draw the symbol for the circuit in Question 18.
- 20. (4 Points) Draw the gates to implement the circuit in Question 18.
- 21. (8 Points) Draw a circuit diagram showing the logic in the leftmost slice of the ALU designed in the book. Include the logic to generate the condition code values. (Carry, oVerflow, Negative, and Zero; for Zero draw the gate and write a note about where most of the inputs come from.)
- 22. (4 Points) Put a checkmark next to each combination of <u>Carry and Overflow that is possible when</u> doing two's complement addition or subtraction. Leave impossible combinations blank.

С	V	Possible?
0	0	
0	1	
1	0	
1	1	

23. (4 Points) In Java, C, and C++, 101011 & 011001 = ? (Circle the *best* choice.)

A. true

- B. false
- C. 001001
- D. 111111
- E. 110110
- 24. (4 Points) Draw a timing diagram that shows the behavior of a D flip-flop in response to three clock pulses. The first pulse is to turn the flip-flop on, the second one is to leave it on, and the third one is to turn it off. Include Clock, D, and Q signal lines in your diagram.
- 25. (4 Points) Draw the symbol for a D flip-flop and add circuitry that will make its state toggle every time there is a clock pulse.