NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS: Answer all questions in your examination booklet, *in sequence, please.* Unless otherwise indicated, all questions count equally.

NEATNESS, LEGIBILITY, AND ENGLISH USAGE ALL COUNT!

1. Name each of the stages in the pipelined register design developed in the textbook. For each stage, tell what that stage does. Answer the question in the same order as the stages are used. To show you what you are to do, here is the answer for the first (leftmost) stage. You do not need to copy this answer to your exam book:
   > "Instruction Fetch Stage. Uses the address in the PC to read the next instruction from the Instruction Memory."

2. For the pipeline design without register forwarding, list the names of each pipeline register, and for each pipeline register tell the fields within the register, how wide each field is (number of bits), and what information is in that field. To help you, here is the answer for the *second* pipeline register:
   > "ID/EX. Control bits: Write Back (2 bits: RegWrite, MemtoReg); Mem (3 bits: Branch, MemRead, MemWrite); Ex (4 bits: RegDst, $ALUOp_1$, $ALUOp_0$, ALUSrc); PC+4 (32 bits); ReadData_1 (32 bits); ReadData_2 (32 bits); SignExtImm (32 bits); rt (5 bits); and rd (5bits)."

   Remember, the answer above is for the second stage; you have to start with the first stage. You do not need to copy this answer for the second stage to your exam book.

3. The instruction *add $6, $3, $2* is at memory address 100_{ten}. What would be the contents of all the fields in the ID/EX register when this instruction reaches it? Assume every register contains the value 10_{ten} plus the register number and that every word of data memory contains 1000_{ten} plus the byte address of the memory word. *Note:* The function code for *add* instructions is 32_{ten}.

4. Explain how *cost*, *capacity*, and *access time* relate to the structure of a *memory hierarchy*.

5. Tell what makes the hard disk so different from the other layers of a memory hierarchy. Then describe the components of access time for a hard disk.

6. A cache memory is 1% of the size of main memory, yet the hit ratio is observed to be 0.97. Explain why a naïve assumption would be that the hit ratio would be 0.01 and explain why such a high hit ratio is actually a reasonable expectation.

7. Main memory consists of 2^{32} bytes, but is accessed one word (four bytes) at a time. The memory system has a 4-way set associative cache with 512 sets. Each cache line holds 256 bytes. Show all work and label all values for partial credit.
   A. How many bits are there in the *tag*, *index*, *block offset*, and *word offset* fields of a memory address?
   B. How many data bits are there in each cache line?
   C. There is a V (valid) bit, but no D (dirty) bit for each cache line.
      a. Does the cache use a *write back*, or a *write through* policy?
      b. What is the total number of bits in each cache line?
   D. Ignoring housekeeping bits that might be introduced for implementing the replacement policy (LRU, etc.), what is the total number of bits in each set?
   E. What proportion of main memory can fit in cache? (You can answer as a power of two. That is, if the answer is ¼, you can say 2^{-2} rather than 0.25.)
   F. What is the total size of the cache in bits? You don't have to do the actual arithmetic; just show what numbers are involved in the calculation. That is, you could write "(3+2)*5" instead of "25".)