

NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

-- INSTRUCTIONS --

- For multiple choice questions, circle the answer of the best choice.
- Draw diagrams on the backs of the exam sheets, making sure you indicate the question number clearly next to each diagram.
- For other questions, follow the directions given in the question.

1. How many rows are there in a truth table with m input variables and n output variables?
 - A. m
 - B. n
 - C. $m + n$
 - D. 2^m
 - E. $2^m \times 2^n$
2. How many columns are there in a truth table with m input variables and n output variables?
 - A. m
 - B. n
 - C. $m + n$
 - D. 2^m
 - E. $2^m \times 2^n$
3. What is the period of a 1 GHz clock?
 - A. 1 millisecond
 - B. 1 microsecond
 - C. 1 nanosecond
 - D. 1 picosecond
 - E. 0.0001 second
4. What is the frequency of a clock with a period of 500 picoseconds?
 - A. 500 GHz
 - B. 50 GHz
 - C. 5 GHz
 - D. 0.5 GHz
 - E. 2 GHz
5. How many propagation delays are needed to implement an arbitrary (unminimized) boolean function using AND, OR, and Inverter gates?
 - A. It depends on the number of rows in the truth table.
 - B. It depends on the number of OR gates.
 - C. It depends on the number of AND gates.
 - D. It depends on the number of input variables.
 - E. 3
6. What is the difference between a boolean *variable* and a boolean *literal*?
 - A. They are the same thing.
 - B. There are two literals for each variable: its complemented and not-complemented forms.
 - C. A variable is an input, but a literal is an output.
 - D. A literal is an input, but a variable is an output.
 - E. Variables correspond to AND gates, but literals correspond to XOR gates.
7. What is the result of the XOR of a variable with a constant?
 - A. The value of the constant.
 - B. The complement of the constant.
 - C. If the constant is 0, the result is the same as the variable; if the constant is 1, the result is the complement of the variable.
 - D. The two's complement of the minuend.
 - E. The one's complement of the multiplier subtracted from the two's complement of the quotient.

8. How can you tell if a two's complement number is negative?
- If the leftmost bit is zero.
 - If the rightmost bit is zero.
 - If the leftmost bit is one.
 - If the leftmost bit is zero.
 - If the middle bit is either zero or one.
9. How is two's complement subtraction accomplished?
- Add the two operands and negate the result.
 - Negate both operands and add.
 - Invert both operands and add.
 - Invert the first operand, negate the second operand, and add.
 - Negate the second operand and add.
10. What is the weight of the leftmost bit of an n -bit two's complement number?
- $+2^n$
 - $+2^{n-1}$
 - $+2^{n+1}$
 - -2^{n-1}
 - -2^{n+1}
11. Which statement is true about Carry and Overflow for two's complement addition?
- They are the same thing.
 - If the carry out of the leftmost position is 1, there is overflow.
 - If the carry out of the leftmost position is 0, there is no overflow.
 - If the carry into the rightmost position is the same as the overflow, the carry out of the leftmost position will be the same as the carry into the second position from the right, which will be the opposite of the carry out of the rightmost position unless the overflow bit was reset by the operating system during the previous two successive invocations of the square root function.
 - The carry out of the leftmost position can be either the same as the overflow bit or not.
12. How is *Bnegate* implemented in the MIPS ALU?
- Invert the bits of the A operand.
 - Invert the bits of the B operand.
 - Invert the bits of both the A and the B operands.
 - Invert the bits of the B operand, and make C_0 true.
 - Connect *SLTin* to *SLTOut*.
13. Fill in the un-shaded blanks in this table for the four-bit implementation of the MIPS ALU. Everything is hexadecimal. The last row is for extra credit.

A	B	Function	CVNZ	Result
0	0	0		
5	3	1		
0	0	2		
0	0	6		
5	3	2		
E	E	2		
7	8	2		
E	E	6		
F	3	7		
3	2	C		

14. Draw a diagram that shows the relationships among the following components of a Finite State Machine (FSM): *external inputs*, *external outputs*, *combinational logic*, *flip-flops*, *present state*, *next state*.
15. Draw the symbol for a positive edge-triggered D-type flip-flop. Mark the C, D, and Q inputs/outputs in the usual way, and label the wires that carry the *present-state* and *next-state* information.
16. Draw a state diagram (circles and arrows) for a FSM with three states named *State_0*, *State_1*, and *State_2*. The FSM cycles through the three states in 0, 1, 2, 0, ... order whenever an external input named *run* is true, and does not change state whenever *run* is false. There is an external output named *Zero* that is true when the FSM is in *State_0* and false otherwise.
17. How many flip-flops would be needed to implement the FSM in Question 16?
 - A. 0
 - B. 1
 - C. 2
 - D. 4
 - E. 8
18. Draw the truth table for the combinational logic portion of the FSM in Question 16.
19. How many of each of the following items are there on a DE1? Count only the items that are available for use as inputs and outputs on the FPGA.
 - A. _____ Red LEDs
 - B. _____ Green LEDs
 - C. _____ Seven Segment Displays
 - D. _____ Slide Switches
 - E. _____ Push Buttons
20. Use a Karnaugh Map to minimize the *Cout* function of a full adder. Show all work.
21. Draw a schematic diagram showing the AND, OR, and Inverter gates to implement a 4×1 multiplexer.