NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS: ***Unless stated otherwise, circle the letter of the one best choice for multiple choice questions. Draw diagrams on the back of the exam sheets. Answer other questions as indicated. Point values given for each question are estimated relative weights: they may be changed (in the case of a bad question, for example), and they do not add up to 100.***

1. (4 points) What is the difference between *sequential* and *combinational* logic?
   A. *Combinational logic* is made by combining sequential circuits.
   B. The values of the inputs to a *sequential logic* circuit completely determine the values of the outputs, but a single set of input values to a *combinational logic* circuit can produce different output values at different times.
   C. The values of the inputs to a *combinational logic* circuit completely determine the values of the outputs, but a single set of input values to a *sequential logic* circuit can produce different output values at different times.
   D. Both do the same things, but *combinational logic* is faster than *sequential logic*.
   E. Both do the same things, but *sequential logic* is less expensive than *combinational logic*.

2. (4 points) Why can't latches be used to implement finite state machines (FSMs)?
   A. They are too expensive.
   B. They are too slow.
   C. They are too large.
   D. They can change state multiple times during a clock pulse.
   E. They require both positive and negative clock edges in order to work reliably.

3. (4 points) Draw a schematic diagram showing how to construct a clocked D *latch* (not a *flip-flop*) using AND, NOR, and NOT gates. Label all inputs and outputs. *Answer on the back of an exam sheet; be sure to put this question number (3) next to your answer.*

4. (4 points) For a D-type flip-flop:
   A. The present state is the value of Q and the next state will be whatever the input value to D is.
   B. The present state is D and the next state is Q.
   C. The present state and the next state are always the same.
   D. The values of D and Q are always the opposite of each other.
   E. The clock output has to be connected to the Q input.

5. (4 points) Draw the diagram that shows the relationships among *flip-flops*, *the clock*, *external inputs*, *external outputs*, *combinational logic*, *present state*, and *next state* for the FSM model. Be sure to indicate each of the underlined terms on the diagram. *Answer on the back of any exam sheet; write this question number (5) next to your diagram.*

6. (4 points) When do FSM *state transistions* occur? (*Technicality: there are different types of FSMs that might allow a different answer to this question. This question is for the "Moore Machine" designs we worked with in this course.*)
   A. Whenever the inputs change.
   B. Whenever the outputs change.
   C. When the inputs and outputs are different from each other.
   D. When the next state is the same as the present state.
   E. When there is a clock pulse.

7. (4 points) How are FSM *state transitions* indicated on a state diagram?
   A. By circles
   B. By arcs connecting circles
   C. By a symbol above the horizontal line inside the circles
   D. By symbols below the horizontal line inside the circles
   E. By the letters *S.T.* or *s.t.* next to the circles.

8. (8 points) Complete this truth table for the combinational logic part of a FSM that operates as a *modulo-8 up counter*. There are no external inputs, but there is an exteral output named Z that is to be true when the counter is in State 0. *Do not implement the truth table.*

present state			next state			output
S_2	S_1	S_0	S_2	S_1	S_0	Z
0	0	0				
		1				
		0				
		1				
		0				
		1				
		0				
		1				

9. (4 points) How many bits are associated with each port of the MIPS memory file?
   A. 5: the register number
   B. 32: the register data
   C. 37: the sum of (A) and (B)
   D. 64: the two read data values
   E. 96: the two read data values plus the write data value

10. (8 points) Circle the letters of *all the true items* in this list:
   A. Register 0 has the same number of flip-flops as all the other registers.
   B. Register 0 has half as many flip-flops as all the other registers.
   C. Register 0 has twice as many flip-flops as all the other registers.
   D. The clock inputs of all the flip-flops in a register are connected together.
   E. The D inputs of all the flip-flops in a register are connected together.
   F. The Q outputs of all the flip-flops in a register are connected together.
   G. The D inputs of all the flip-flops in a single *bit-slice* (column) of the register file are connected together.
   H. The Q outputs of all the flip-flops in a single *bit-slice* (column) of the register file are connected together.
   I. It is possible to read the same register out of both read ports at the same time.
   J. It is possible to write to the same register that is being read from in the same clock cycle.
   K. Writing to register zero has no effect.

11. (8 points) Draw a diagram showing how one flip-flop in the MIPS register file connects to the three ports. Include block symbols for the decoder and multiplexers; show how the clock is connected. *Answer on the back of any exam sheet; write this question number (11) next to your diagram.*

12. (4 points) What are the factors that determine the CPU execution time of a program?
   A. The instruction set architecture, the amount of memory, and the number of propagation delays.
   B. The clock speed, the amount of memory, and the instruction set architecture.
   C. The instruction count, the average number of clocks per instruction, and the clock cycle time.
   D. The instruction count, the instruction set architecture, and the amount of memory.
   E. The number of propagation delays, the clock speed, and the clock cycle time.

13. (8 points) Two computers, A and B, execute the same program. Computer A has 2 GB of RAM, a clock speed of 1 GHz, requires an average of 2 clock cycles per instruction, and executes 1,000,000,000 instructions when running the program. Computer B has 4 GB of RAM, a 2 GHz clock speed, requires an average of 3 clock cycles per instruction, and executes 1,500,000,000 instructions when running the program. *Fill in the blanks:*
   A. How long does it take Computer A to complete the program? _____ seconds.
   B. How long does it take Computer B to complete the program? _____ seconds.
   C. Computer _____ is _____ times faster than computer _____, which is the same as saying it is _____% faster.

14. (8 points) Assume register $a0 contains 0x00001000. Write a sequence of MIPS assembly language instructions that adds the contents of the two memory words at addresses 0x00001000 and 0x00001004 together and stores the sum in memory word 0x00001008. *Answer here:*

15. (8 points) Name and give the *binary* contents of each field of the machine language representation of this instruction:

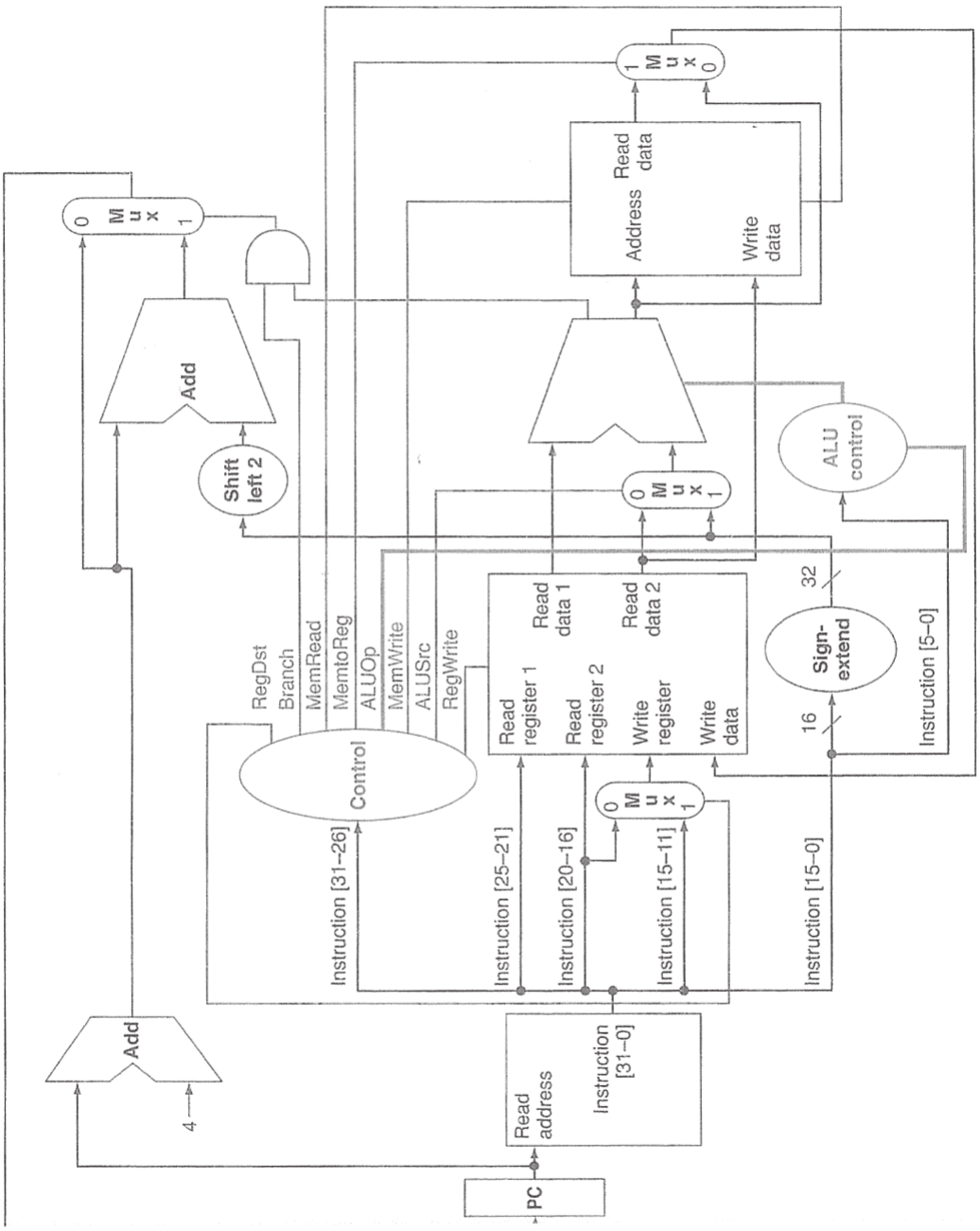
    or $15, $10, $3

    (*Hint: register 15 is the one that gets the result.*) *Answer here:*

16. (4 points) Circle the letters of *all* the uses of I format instructions:
    A. Branching
    B. Arithmetic using two registers for operands
    C. Jumping
    D. Arithmetic using one register and an immediate value for operands
    E. Memory loads and stores

17. (8 points) *0x10E9FFFC* is a branch instruction.
    A. The *op code* in binary is: _____
    B. The mnemonic for the op code is _____
    C. The *rs* register number is: _____
    D. The *rt* register number is: _____
    E. The *BranchAddr* (see footnote 4) is: _____ Answer in hexadecimal.

18. (8 points) *On the diagram on the next page:*
    A. Write *ALU*, *Data Memory*, *Instruction Memory*, and *Registers* in the corresponding boxes. You may use *DM, IM, and Regs* to abbreviate the last three.
    B. Label the line that has the value *PC+4*.
    C. Label the *Zero* condition code bit.
    D. Add the missing parts needed to implement Jump (*j*) instructions.


M u x
0
1
Add
4
Shift left 2
Address
Read data
Write data
ALU control
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Control
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
32
Sign-extend
16
Instruction [5–0]
Instruction [31–26]
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Read address
Instruction [31–0]
PC