NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS: Answer questions in the spaces provided; circle the choice of the best answer for multiple choice questions Longer questions count more than shorter ones. *Show all work for partial credit.*

Questions marked * must include the correct unit of measure to receive full credit.

NO CALCULATORS OR OTHER ELECTRONIC DEVICES.

1 Is it all right to use a calculator or any other electronic device on this exam? (Read the instructions above, then choose the best answer.)
A. No, it says NO CALCULATORS in the instructions.
B. I want to get this question wrong.

2. 5,400 Revolutions Per Minute (RPM) is _____ revolutions per second.

3. 5,400 RPM is _____ seconds per revolution.

4. Convert your answer to Question 3 to milliseconds: _____ msec

5. Convert your answer to Question 3 to microseconds: _____ µsec.

6. Define the four components of disk access times and give representative ranges of values for each. *

7. Define the three parameters that characterize the layers of the memory hierarchy, and tell whether each one *increases* or *decreases* as the layers get closer to the CPU.

8. What are L1 and L2?
A. Cache levels; L1 is normally part of the CPU and L2 is normally external to it.
B. Cache levels; L2 is normally part of the CPU and L1 is normally external to it.
C. Parts of the virtual memory system managed by the operating system.
D. The states in which an instruction is fetched and decoded, respectively.
E. The first two stages of a pipelined CPU.

9. What do *write through* and *write back* refer to?
A. Mechanisms for reducing disk access time.
B. Mechanisms for managing the clocks per instruction (CPI) of a pipelined processor.
C. Mechanisms for managing the CPI of a multi-cycle processor.
D. Mechanisms for managing memory write operations in a cache system.
E. Mechanisms for managing the memory map registers in a virtual memory system.

10. A memory has 2^{30} words of byte addressable memory, with four bytes per word. There are 2^{12} cache lines, and each cache line holds 2^5 words of memory.
    A. How many bits are needed for each memory address: _____ bits
    B. How many bits are used to select a byte within a word: _____ bits
    C. How many *bytes* of memory are in each cache line? _____ bytes
    D. How many *blocks* of main memory are there? (1 block = 1 line) _____ blocks
    E. What is the maximum proportion of main memory that can be in cache at a time? _____
    F. How many address bits are used to select a word from a cache line? _____ bits
    G. For a direct mapped cache, how many address bits are used for the *index* field? _____ bits
    H. For a direct mapped cache, how many address bits are used for the *tag* field? _____ bits
    I. For an 8-way set associative cache, how many address bits are used for the *index* field? _____bits
    J. For an 8-way set associative cache, now many address bits are used for the *tag* field? _____ bits

11. Main memory has an access time of 50 nsec. The CPU clock speed is 2 GHz and an L2 cache requires two CPU clock cycles per access.
    A. What is the time to access L2? * _____
    B. What is the average access time if the L2 hit ratio is 0.90? * _____
    C. Assuming the design in Question 10, what must the *bandwidth* between main memory and L2 be in order to support an access time of 50 nsec? (*Hints: (1) Remember that each access fetches 2^5 words and there are 2^2 bytes per word. (2) Bandwidth is a* rate *measure.*) *_____

12. A single-cycle CPU design uses a 200 MHz clock. If the CPU were implemented using a perfectly balanced 5-stage pipeline, what would the pipelined clock *speed* (frequency) be? *_____

13. What would be the *latency* of a 10-stage pipeline using a 5 GHz clock? *_____

14. What information is passed through the IF/ID pipeline register in the processor design used in Chapter 6 of the textbook? (*Hint: two fields.*)

15. What information is passed through the MEM/WB pipeline register in that processor design? (*Hint: two control bits and three other fields.*)

16. What is a *data hazard?*

17. What is a *control hazard?*

18. What is *register forwarding?*

19. Intel has been criticized for using very deep pipelines (20 stages or more) in order to increase processor clock speed as a marketing ploy. Ignoring the marketing issue, and considering the topics in Questions 13 and 17, why might a very deep pipeline lead to poorer performance than a shallower pipeline?