NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS: For multiple choice questions, circle the letter of the *one best choice* for each question. There is no penalty for guessing. For other questions, follow the directions in the question. Questions 9, 10, 17, and 25 count twice as much as the multiple choice questions..

1. What is the main feature of the DE-1 logic kits that prevented us from implementing the full 32-bit MIPS ALU on them?
   A. The kits are too slow.
   B. The FPGAs on the kits are too small to hold an entire ALU.
   C. There not enough inputs (buttons and switches) and outputs (LEDs and Seven segment displays) to enter and display 32-bit values easily.
   D. The carry-lookahead units on the kits are broken.
   E. There was no problem with the kits; the problem was that *Quartus* can generate a full 32-bit ALU only using Verilog, not using schematics.

2. What statement best describes the purpose of the *MIPS_ALU_Testbed.v* file that I supplied?
   A. It generated test vectors so that the simulator could verify the correctness of the program.
   B. It downloaded the configuration file to the FPGA.
   C. It provided a Verilog implementation of the complete project so that we would know how the full adder and bit slice modules were supposed to work.
   D. It let us know that Dr. Vickery cared enough to do the project himself.
   E. It provided the interface between the DE-1 inputs and outputs and the MIPS_ALU module.

3. What is the essential difference between `MIPS_ALU.v` and `MIPS_ALU.bdf`?
   A. They are two different ways to generate equivalent logic circuits using a hardware description language and a schematic diagram, respectively.
   B. The `.v` file just tells how to draw a symbol for the ALU, but the `.bdf` file tells how to implement it.
   C. The `.v` file uses flip-flops and XOR gates to implement the ALU, but the `.bdf` file uses AND, Nor, and OR gates.
   D. The `.v` file is bigger than the `.bdf` file.
   E. The `.v` file has to be simulated, but the `.bdf` file has to be interpreted.

4. What is a `.bsf` file?
   A. A schematic diagram.
   B. A Verilog program module.
   C. A symbol for a module that can be placed in a schematic diagram.
   D. A *Binary System Format* object.
   E. A list of errors that occur during compilation.

5. What role did the *Quartus* "Add/Remove Project Files" menu item play in the MIPS_ALU assignment?
   A. It was used to generate the file for programming the FPGA.
   B. It was used to add symbols to a schematic diagram.
   C. It was used to specify the part number of the FPGA used in the project.
   D. It was used to remove the Verilog version and add the Schematic Diagram version of each module implemented in the assignment.
   E. It was not necessary to use this menu item in the assignment.

6. What is a LED?
   A. A *Luminescent Extraction Device*
   B. A *Less-than or Equal Dectector*
   C. A *Left-End Divider*
   D. A *Limited Event Doubler*
   E. A *Light Emitting Diode*

7. What was Switch 9 used for in the Up/Down counter project?
   A. To set the number of states
   B. To select the free-running or manual clock source
   C. To reset the project
   D. To download the project into the FPGA
   E. To turn the seven segment displays on or off.

8. What were the right two Key (pushbutton) inputs used for in the Up/Down Counter project?
   A. To set the number of states
   B. To select the free-running or manual clock source
   C. To cause the counter to count up or down
   D. To turn the red LEDs on and off
   E. To set the speed of the free-running clock

9. On the back of this sheet, draw a diagram showing the elements of the Finite State Machine model for the modulo-4 up/down counter project. Label the combinational logic and state register sections; show where the clock connects; label the present state and next state signals, and indicate how many wires are in each; label the external inputs and outputs. Be sure to mark your answer "Question 9."

10 . On the back of this sheet, draw a diagram showing the complete state diagram for the modulo-4 up/down counter project. Label each circle with a meaningful state name; show the external output(s) that are true inside the circle for each state; label each arc with the values of the variable(s) that cause the transition. Be sure to mark your answer "Question 10."

11. What causes transitions from one state to another in a Finite State Machine?
   A. When you download the project from the computer to the FPGA
   B. When you upload the project from the FPGA to the logic kit
   C. When the seven segment displays change value
   D. When the system is reset
   E. When there is a clock pulse

12. What part of the FSM model is designed using a *State Table* ?
   A. The state register
   B. The combinational logic
   C. The clock circuit
   D. The arc lengths
   E. The state names

13. What is the difference between *Mealy* and *Moore* outputs of a FSM?
   A. The Mealy outputs are the inputs to the Moore outputs.
   B. The Moore outputs are the inputs to the Mealy outputs.
   C. The Mealy outputs are true, but the Moore outputs are false.
   D. The Mealy outputs are red, but the Moore outputs are blue.
   E. Moore outputs depend only on the current state; Mealy outputs depend on both the current state and the values of the external inputs.

14. Why can't level-sensitive flip-flops (latches) be used to construct FSMs?
   A. Because they cost too much.
   B. Because they are too slow.
   C. Because they are too fast.
   D. Because they can change state during a clock pulse.
   E. Because they don't hold enough information to represent the states.

15. What is the *ENA* input of a D flip-flop used for?
   A. To turn it on
   B. To turn it off
   C. To make it toggle
   D. To connect it to the Clock inputs of the other flip-flops of the same register
   E. To enable or disable clock pulses from affecting the flip-flop without causing clock skew

16. What is different about *PRN* and *CLRN* compared to the *D* input of a D flip-flop?
    A. They operate independently of the clock.
    B. They can only be used to connect the flip-flop to other flip-flops, but D can be used to reset it.
    C. They use more power.
    D. They expand the number of bits of information the flip-flop can hold.
    E. They are red and blue instead of green.

17. On the back of this sheet, draw **all the gates** to implement an edge-triggered D flip-flop with *ENA*. You may make your flip-flop either positive or negative edge-triggered *Bonus: tell (correctly!) whether your flip-flop is positive or negative edge triggered.* Be sure to mark your answer "Question 17." **Note:** You must draw all the gates, not just symbols for latches.

18. What do all the flip-flops in a register have in common?
    A. Their D inputs are connected together.
    B. Their Clock inputs are connected together.
    C. Their Q outputs are connected together.
    D. Their D outputs are connected together.
    E. Their Q inputs are connected together.

19. Which operation puts information into a register?
    A. Register Read
    B. Register Write
    C. Both *Register Read* and *Register Write*
    D. *CVNZ*
    E. All of the above

20. What is special about Register 0 in the MIPS processor?
    A. Nothing special; it is just like all the others.
    B. If a program tries to write to it, the CPU will print an error message.
    C. If a program tries to read from it, the CPU will print an error message.
    D. Writing to it does nothing; reading from it always gets the value `0x00000000`.
    E. It serves as a source of random numbers.

21. How many wires are needed for each read and write port of the MIPS register file?
    A. 2^{32}
    B. 37: 5 for the register number, plus 32 for the data
    C. 64: 32 for the register number, plus 32 for the data
    D. 37: 32 for the register number, plus 5 for the data
    E. None: it is a wireless hot spot

22. How many operations can the MIPS register file perform per clock cycle?
    A. One: either a *read*, or a *write*.
    B. Two: one *read* and *one write.*
    C. Three: two *reads* and one *write.*
    D. Three: one *read* and two *writes.*
    E. Four: two *reads* and two *writes*.

23. How many gates are there in a 32×1 multiplexor?
    A. Five inverters and 32 AND gates
    B. Five inverters, 32 AND gates, and one OR gate
    C. 32 inverters, 32 AND gates and one OR gate
    D. 32 inverters, one AND gate and 32 OR gates
    E. None: multiplexors are made out of flip-flops, not gates

24. How many gates are there in a 32×32 multiplexor?
    A. 32 inverters and 32 AND gates
    B. 32 inverters, five AND gates, and 32 OR gates
    C. Five inverters, 1,024 AND gates, and 32 OR gates
    D. 1,024 inverters, 1,024 AND gates, and 1,024 OR gates
    E. Three clocks, two flip-flops and 32 XOR gates

25. In the space below, draw a diagram that shows how register write operations are implemented in the MIPS register file. Use symbols for 2-3 representative registers. Assume the flip-flops have *ENA* inputs. Be sure to show the how the ALU results connect to the registers, how the Write Register number selects the register to be written, and how the clock input is connected to the registers. Be sure to label the inputs and outputs of the decoder accurately.