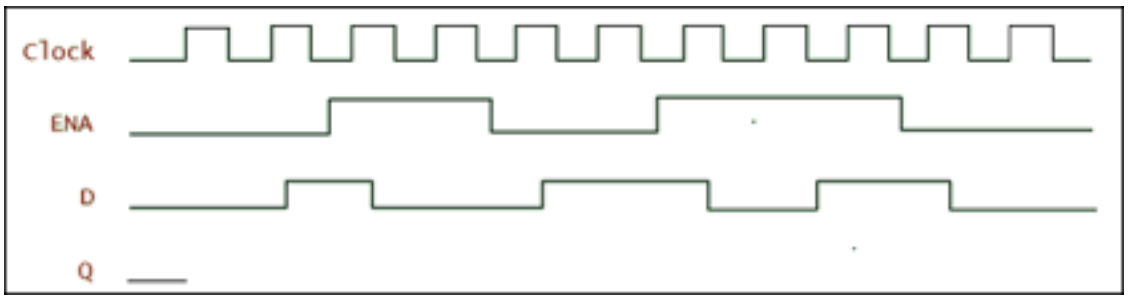
First Name Last Name **CS-343 Exam 2** **April 7, 2009**
Student ID: Student ID Exam ID: Exam ID

Instructions:

- Draw diagrams on the backs of the exam sheets or after the last question. *You must put the question number next to each diagram to receive <u>any</u> credit for them.*
- Answer other questions in the spaces provided.
- Unless otherwise indicated, all questions count equally.

1. Draw a schematic diagram for an unclocked R-S latch using NOR gates. Label all inputs and outputs meaningfully.
2. Draw a schematic diagram for a clocked R-S latch using AND and NOR gates. Label all inputs and outputs meaningfully. Do not include an ENA input.
3. Draw a schematic diagram for a clocked D latch using AND, NOR, and NOT gates. Label all inputs and outputs meaningfully. Do include the ENA input.
4. Draw a symbol to represent your schematic from Question 3. Label all inputs and outputs meaningfully.
5. Use your schematic from Question 4, plus whatever other gates are necessary to construct a schematic for a positive edge-triggered D flip-flop.
6. Complete this timing diagram for a positive edge-triggered D flip-flop. Answer here:



7. Draw a single symbol for the entire MIPS register file used in the book. Label all inputs and outputs meaningfully, and indicate how many wires connect to each input or output.
8. Draw all the gates in a 4×2 multiplexer. Label all inputs and outputs meaningfully.
9. Using a symbols for positive edge-triggered D flip-flops with enable and for whatever multiplexers and decoders are needed, draw a schematic diagram for a 4×2 register file with one read port and one write port. Label all inputs and outputs meaningfully.
10. Describe in English how the target address of a conditional branch instruction is calculated:

11. Write the Verilog expression corresponding to the answer to Question 10.

12. Describe in English how the effective address is calculated for *lw* and *sw* instructions is calculated:

13. Write the Verilog expression corresponding to the answer to Question 12.

14. What is the op code of all R-Format instructions, in binary:
15. Draw diagrams for the R, I, and J MIPS instruction formats. Show the names and number of bits in each field of each format; be sure to indicate which format is which.

16. Tell what the *RegDst* control signal is used for. *Help: this is the signal that controls the mux between instruction memory and the register file.*

***RegDst* Value**	**Effect**
0	
1	

17. For each instruction format tell whether *RegDst* is normally 0, 1, or X. Be sure your answers are consistent with your answers to the previous question. (*Don't think too hard about this; there are examples of all three formats where RegDst can be X; just give the value that is most commonly appropriate for each format.*)

Instruction Format	***RegDst* Value (0, 1, or X)**
R	
I	
J	

18. What is *random* about a Random Access Memory?

19. What binary property do all MIPS *instruction addresses* have in common with each other?

20. Name the two elements of the MIPS single-cycle datapath that are connected to the datapath clock:

21. What determines the minimum allowable period for the MIPS single-cycle datapath clock? Be as specific as you can.

22. Name the connections to an edge-triggered D flip-flop that correspond to the flip-flop's *present state* and *next state.*

End of Questions