First Name Last Name
Student ID: Student ID

CS-343 Exam 2

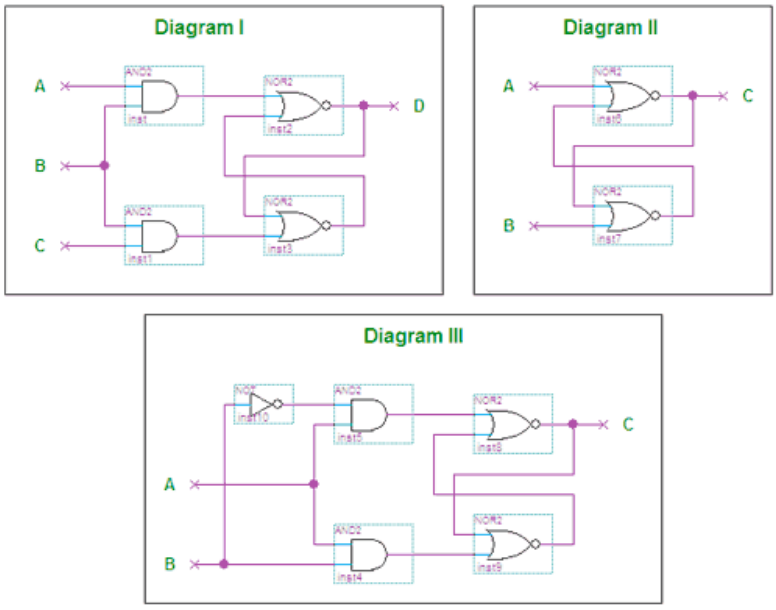
November 10, 2009
Exam ID: Exam ID

Instructions:

- For multiple choice questions, circle the letter of the one best choice unless the question explicitly states that it might have multiple correct answers.
- There is no penalty for guessing.
- Place drawings where indicated in the question; be sure to put the question number next to your drawing; use pencil rather than ink.
- Diagrams count more than short answer questions.

1. Can you use a truth table to describe the behavior of a sequential circuit?
   A. Yes: as long as *clock* is one of the inputs, a truth tables describe the behavior of sequential circuits just as fully as they describe combinational circuits.
   B. Yes: because sequential circuits are actually constructed using combinational circuits, there is no essential difference between the two, and truth tables describe sequential circuits perfectly well.
   C. Yes: Truth tables list the values of all output variables for every possible combination of input variables, which is exactly what is needed for describing the behavior of sequential circuits.
   D. Yes: Truth tables and finite state machines are actually two names for the same thing.
   E. No: Sequential circuits can have different output values for a particular combination of input values, making truth tables inappropriate for describing their behavior.
2. The time from one rising edge of a clock pulse to the next rising edge is called:
   A. The *frequency*, and it is measured in *Hertz.*
   B. The *period,* and it is measured in *Hertz.*
   C. The *frequency,* and it is measured in *seconds.*
   D. The *period,* and it is measured in *seconds.*
   E. The *length*, and it is measured in *meters.*

Questions 3-9 are based on the following diagrams:



3. What is the *name* of the circuit in **Diagram I**?
   A. An unclocked R-S latch
   B. A clocked R-S Latch
   C. An unclocked D Latch
   D. A clocked D Latch
   E. A positive edge-triggered D flip-flop
4. What is the *name* of the circuit in **Diagram II**?
   A. An unclocked R-S latch
   B. A clocked R-S Latch
   C. An unclocked D Latch
   D. A clocked D Latch
   E. A positive edge-triggered D flip-flop
5. What is the *name* of the circuit in **Diagram III**?
   A. An unclocked R-S latch
   B. A clocked R-S Latch
   C. An unclocked D Latch
   D. A clocked D Latch
   E. A positive edge-triggered D flip-flop
6. Fill in the names of the inputs and outputs in **Diagram I**
   A. _____
   B. _____
   C. _____
   D. _____
7. Fill in the names of the inputs and outputs in **Diagram II**
   A. _____
   B. _____
   C. _____
8. Fill in the names of the inputs and outputs in **Diagram III**
   A. _____
   B. _____
   C. _____
9. What do diagrams I, II, and III have in common? **Circle <u>all</u> correct answers.**
   A. They are all sequential circuits
   B. They are all inappropriate to use in finite state machine designs
   C. They are all appropriate to use in finite state machine designs
   D. They are all combinational circuits
   E. They all have the same number of propagation delays
   F. They all are flip-flops
   G. They all are latches

10. What property of flip-flops distinguishes them from latches?
    A. Flip-flops will never change state more than once per clock cycle, but latches can change state multiple times during a clock pulse.
    B. Latches will never change state more than once per clock cycle, but flip-flops can change state multiple times during a clock pulse.
    C. Latches are combinational circuits, but flip-flops are sequential circuits.
    D. Flip-flops are combinational circuits, but latches are sequential circuits.
    E. Flip-flops are faster than latches.
    F. Flip-flops are tastier than latches.
11. In a state diagram (circles and arcs), the *circles* represent:
    A. Inputs
    B. Outputs
    C. Clock signals
    D. States
    E. The D outputs of the latches
12. In a state diagram, when are the transitions represented by the *arcs* taken:
    A. When the inputs connect to the outputs
    B. When the outputs connect to the inputs
    C. When there is a clock signal
    D. When the number of states changes
    E. When D outputs of the latches connect to the Q inputs of the flip-flops
13. What is the smallest number of flip-flops that will be needed to implement a finite state machine with *ten states*?
    A. 0
    B. 1
    C. 2
    D. 3
    E. 4
    F. 5
14. What problem does the *enable* input of a D flip-flop solve?
    A. Race conditions when flip-flops go too fast.
    B. Clock skew when gates are inserted in the path of clock signals.
    C. Incomplete reset when clock pulses are too short.
    D. Incomplete reset when clock pulses are too fast.
    E. Not knowing what state a flip-flop is in.
15. On the back of an exam sheet, draw the *symbol* (only the symbol, not the internal structure) of the full MIPS register file (the one designed in the book, not the one from Assignment 4).
    A. Label all inputs and outputs meaningfully
    B. Show the number of bits for each input and output
    C. Mark your answer clearly with this question number (15).

16. On the back of an exam sheet draw the complete implementation of one 4-bit register, like the design from Assignment 4.
    A. Label the input and output pins of the register meaningfully.
    B. Use symbols (not the internal gates) to represent each flip-flop.
    C. Label the inputs and outputs of each flip-flop clearly.
    D. Mark your answer clearly with this question number (16).
17. Tell the two ways to prevent the result computed by the ALU from being saved in any of the registers of the MIPS register file.
    A. _____
    B. _____
18. On the back of an exam sheet draw a 4×3 multiplexer.
    A. Use a symbol to represent each one-output multiplexer; do not draw gates.
    B. Label all inputs and outputs meaningfully.
    C. Use bus nodes wherever possible.
    D. Indicate the number of wires in each bus node.
19. Answer the following questions about a 32M×4 SDRAM chip. If an item is not part of an SDRAM chip, use 0 (zero) as your answer.
    A. Number of Address wires: _____
    B. Number of Data Input wires: _____
    C. Number of Data Output wires: _____
    D. Number of Chip Select wires: _____
    E. Number of Function Code wires: _____
    F. Number of Write Enable wires: _____
    G. Number of Condition Code wires: _____
20. What is the purpose of *tristate* outputs?
    A. They triple the speed of the gates.
    B. They increase the speed of the gates by 200%.
    C. They allow the outputs of gates to be connected together.
    D. They simplify the boolean functions that use them.
    E. They prevent hackers from compromising the security of the system.
21. For the *rs* wires of the MIPS datapath:
    A. How many wires? _____
    B. Where do they come from? _____
    C. Where do they go? _____
22. For the *rt* wires of the MIPS datapath:
    A. How many wires? _____
    B. Where do they come from? _____
    C. Where do they go? _____
23. For the *rd* wires of the MIPS datapath:
    A. How many wires? _____
    B. Where do they come from? _____
    C. Where do they go? _____

24. For the *R[rs]* wires of the MIPS datapath:
    A. How many wires? _____
    B. Where do they come from? _____
    C. Where do they go? _____
25. For the *R[rd]* wires of the MIPS datapath:
    A. How many wires? _____
    B. Where do they come from? _____
    C. Where do they go? _____
26. Assume there is a 4-bit two's complement variable named *a_variable*. Write a Verilog expression to sign extend the value to 8 bits.

27. What are the three possible inputs to the MIPS PC?
    A. _____
    B. _____
    C. _____
28. What do all the possible inputs to the PC have in common, and why?
    A. They all _____
    B. Because _____