First Name Last Name
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CS-343 Final Exam

December 17, 2009
Exam ID: Exam ID

Instructions:

- For multiple choice questions, circle the letter of the one best choice unless the question explicitly states that it might have multiple correct answers.
- There is no penalty for guessing, so answer all questions.
- If you don't see a question number, it's because of a bug in my word processor. There are approximately 37 questions. Maybe 38. Maybe some jokes that don't count.
- Unless otherwise indicated, all questions count equally.

1. `if (R[rs] == R[rt]) PC = PC + 4 + {14{immediate[15]},immediate,2'b0}`
   A. R-type
   B. J
   C. beq
   D. lw
   E. sw
2. What are two ways of preventing the contents of the MIPS register file from changing when there is a clock pulse?
   A. Turn off the power or stop executing instructions
   B. Make RegWrite or MemtoReg false
   C. Make ALUOp or ALUSrc false
   D. Make RegDst or MemWrite false
   E. Make RegWrite false or set the Write register number to zero
3. What binary property do all MIPS instruction addresses have in common?
   A. They all have a 1 in the rightmost position
   B. They all have a 1 in the leftmost position
   C. They all have 1's in the two rightmost positions
   D. They all have a 1's in both the leftmost and the rightmost positions
   E. They all have zeros in the rightmost two positions.
4. Which of these is the Verilog expression for a Jump instruction's target address?
   A. `{PC+4[31:28], address, 2'b0}`
   B. `{16{immediate[15]},immediate}`
   C. `{14{immediate[15]},immediate,1'b0}`
   D. `{16{1'b0},immediate}`
   E. `{6{address[25]},address}`

6. Which of these is the Verilog expression for the effective address of a load word (*lw*) or store word (*sw*) instruction? The effective address is the memory address where the word will be loaded from or stored into.

   A. `R[rs] + {16{immediate[15]},immediate}`

   B. `R[rd] + {16{immediate[15]},immediate}`

   C. `PC + 4 + {16{immediate[15]},immediate}`

   D. `R[rs] + R[rd]`

   E. `R[rs]`

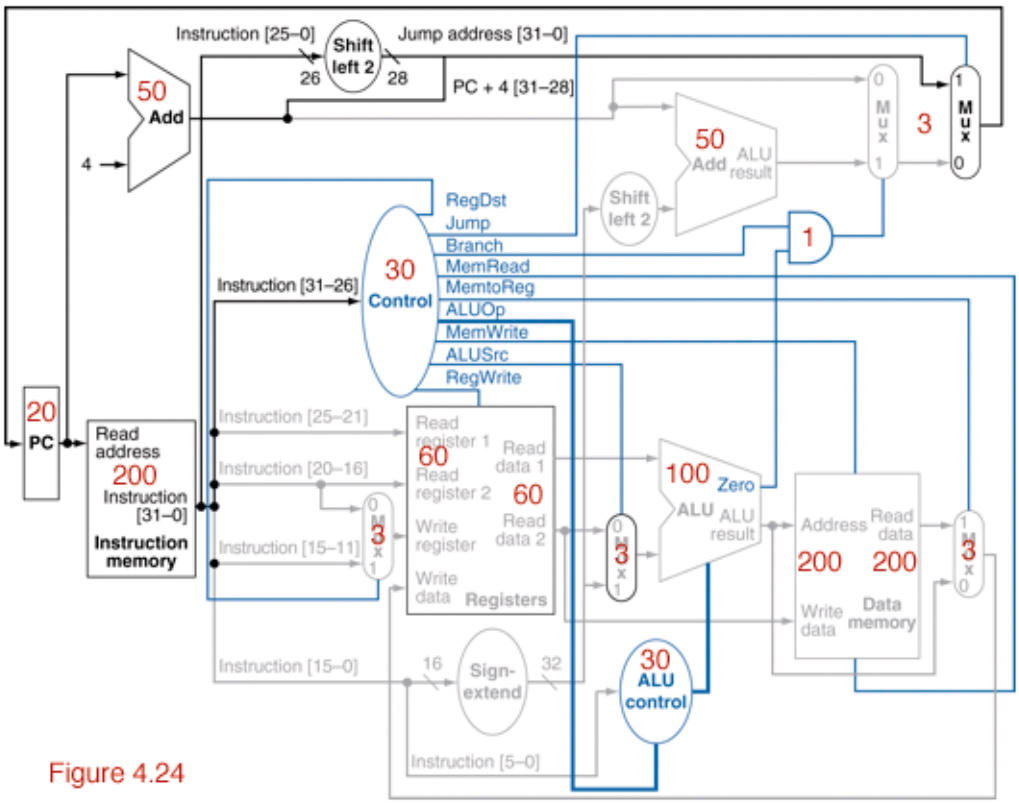

Figure 4.24

The following questions refer to Figure 4.24, above. Give answers as the total number of picoseconds after a clock pulse when the value specified would be valid.

7. The instruction to be executed.

   A. 20 psec

   B. 200 psec

   C. 70 psec

   D. 220 psec

   E. 270 psec

9. The value of PC+4
   A. 20 psec
   B. 50 psec
   C. 70 psec
   D. 200 psec
   E. 270 psec
10. The ALUSrc control signal
   A. 250 psec
   B. 300 psec
   C. 25 psec
   D. 43 psec
   E. 223 psec
11. The `R[rs]` input to the ALU
   A. 280 psec
   B. 310 psec
   C. 60 psec
   D. 63 psec
   E. 93 psec
12. The 4-bit function code input to the ALU
   A. 30 psec
   B. 60 psec
   C. 260 psec
   D. 280 psec
   E. 300 psec
13. The outputs of the ALU (if ALUSrc is 0)
   A. 380 psec
   B. 383 psec
   C. 390 psec
   D. 393 psec
   E. 400 psec
14. The branch target address
   A. 220 psec
   B. 250 psec
   C. 270 psec
   D. 300 psec
   E. The branch target address is never valid
15. For a *lw* instruction, when would the memory word finish being written to the register file? Show all work and indicate where each number in your calculation comes from. You can use the value you chose for outputs of the ALU as your first value.

16. Given your answer to the previous question, what would be the maximum clock frequency this processor could use?
    A. About 1 KHz
    B. About 2.5 MHz
    C. About 1.5 GHz
    D. About 400 msec
    E. About 500 psec
17. If a non-pipelined processor had a maximum clock rate of 500 MHz and was converted to a perfectly balanced 10-stage pipeline, what would the pipelined processor's maximum clock rate be?
    A. 500 nanoseconds
    B. 500 picoseconds
    C. 500 GHz
    D. 50 GHz
    E. 5 GHz
18. For the previous question, what would be the *latency* to execute a single instruction for the non-pipelined processor?
    A. 500 μsec
    B. 500 nsec
    C. 500 psec
    D. 2 psec
    E. 2 nsec
19. What would be the *latency* to execute a single instruction for the pipelined processor?
    A. Same as the previous answer
    B. Some other value
20. What would be the instruction *throughput* for the non-pipelined processor, assuming it uses a single-cycle design like the first part of Chapter 4?
    A. 500 MHz
    B. 500 μsec
    C. 500 nsec
    D. 500 million instructions per second
    E. 500 seconds per million instructions
21. And what would be the instruction *throughput* for the perfectly-balanced 10-stage pipelined design, assuming no hazards?
    A. 500 million instructions per second
    B. 5 billion instructions per second
    C. 5000 seconds per instruction
    D. 50 seconds per instruction
    E. 500 MHz

23. In the pipelined processor developed in chapter 4 of the textbook, in which stage is the *effective address* calculated for *lw* and *sw* instructions?
    A. IF
    B. ID
    C. EX
    D. MEM
    E. WB
24. Circle the letters of *all* the items that would be in the MEM/WB pipeline register:
    A. All the bits of the instruction
    B. The write register number
    C. `{14{immediate[15]},immediate,2'b0}`
    D. The ALU result
    E. The output of data memory
    F. MemtoReg
    G. ALUSrc
    H. PC+4
    I. The *branch* and *jump* control signals
25. What is the problem that *register forwarding* deals with, and how does it do so?

26. What are the three parameters that determine the place of a memory component in a computer's memory hierarchy?
    A. Speed, access time, and latency
    B. Cost, capacity, and volatility
    C. Capacity, dynamics, and packaging
    D. Speed, cost, and capacity
    E. Latency, volatility, and packaging
27. Why are the *tag* bits of a memory address important in a cache memory system?
    A. The more tag bits there are, the higher the hit ratio.
    B. The more tag bits there are, the lower the hit ratio.
    C. The tag bits tell which block of main memory is occupying a cache line.
    D. The tag bits are needed to tell whether a cache line has been modified or not.
    E. The tag bits determine which level of cache is closest to the CPU.

Assume a computer has a byte-addressable memory with 36 bit main memory addresses, and 8 bytes per memory word. It has a 2-way set associative L1 cache with 64K cache lines. There are 32 words per line. It is okay to give answers two raised to an exponent or using standard abbreviations for orders of magnitude (K, M, G, etc). But when asked "how many bits," you have to give the actual number, not an expression.

28. How many bytes of memory? _____
29. How many words of memory? _____
30. How many data bytes per cache line? _____
31. How many data bytes per memory block? _____
32. How many cache sets? _____
33. How many bits for the byte offset (within a word) field of an address? _____
34. How many bits for the word offset (within a block) field of an address? _____
35. How many bits for the index field of an address? _____
36. How many bits for the tag field of an address? _____
37. How many bits for the V-bit of a cache line? _____
38. Did you know that the previous question was a joke? _____
39. Calculate the average number of clock cycles per memory access and the average memory access time for a processor with a one-level cache. The clock speed is 2 GHz, and memory accesses to the cache require one clock cycle. The miss penalty is 5 clock cycles. The hit rate is 0.9. Show all work.

    A. Clock cycles: _____

    B. Access time: _____