Instructions:

- For multiple choice questions, circle the letter of the *one best choice* unless the question explicitly states that it might have multiple correct answers.
- There is no penalty for guessing, so answer all questions.
- Place drawings where indicated in the question; be sure to put the question number next to your drawing; use pencil rather than ink.
- Unless otherwise indicated, all questions count equally.

1. A logic network has $n + 1$ inputs and 2^n outputs; no more than one output is ever true at a time, but it is possible for none of the outputs to be true. What is the name of this network?
   A. multiplexer
   B. register file
   C. decoder
   D. decoder with enable
   E. tristate
2. On the back of an exam sheet, draw all the gates needed to implement the network described in Question 1 for $n = 2$. Label all inputs and outputs meaningfully. Put this question's number next to your answer.
3. How many *select* inputs does a 4×1 multiplexer have?
   A. 1
   B. 2
   C. 3
   D. 4
   E. 5
4. How many *select* inputs does a 4×3 multiplexer have?
   A. 1
   B. 2
   C. 3
   D. 4
   E. 5
5. How many flip-flops are there in the full MIPS register file?
   A. 8×3
   B. 8×4
   C. 7×32
   D. 31×32
   E. 32×32

6. Why is it important to use flip-flops instead of latches to construct a finite state machine?
   A. Flip-flops are the only way to provide the speed necessary for reliable finite state machine operation.
   B. The reduced speed of flip-flops is necessary to ensure reliable finite state machine operation.
   C. Flip-flops cost less than latches, so you have to use flip-flops to obtain the most economical implementation possible.
   D. Flip-flops use less power than latches, so their use is important for optimizing battery life.
   E. Flip-flops will never change state more than once per clock cycle, which is essential for designs like finite state machines where the outputs of the machine feed back into the inputs.
7. On the back of an exam sheet, draw all the gates to implement an *unclocked R-S latch*. Label all inputs and outputs meaningfully. Put this exam question's number next to your answer.
8. On the back of an exam sheet, draw a *symbol* (not the gates and/or flip-flops) for one register of the full MIPS register file using the register used in Assignment 5 as a model, but scaled up to the size of the full MIPS registers. Label *all* inputs and outputs meaningfully. Be sure to put this question's number next to your answer.
9. The full MIPS register file uses a decoder to control which register (if any) gets written to. On the back of an exam sheet draw a *symbol* (not the gates) to show the structure of this decoder. Label all the inputs meaningfully. There are too many outputs to draw them all carefully, but make it clear exactly how many there are, and indicate where they all go. For example, you could label just one output with a phrase like, " to the __ input of __." Be sure to put this question's number next to your answer.
10. Which of the following differentiates between *static* (SRAM) and *dynamic* (DRAM) memories?
    A. SRAM is read-only, but DRAM can be both read and written.
    B. SRAM has less capacity, costs more per bit, but is faster to access than DRAM.
    C. DRAM has less capacity, costs more per bit, but is faster to access than SRAM.
    D. SRAM uses static electricity, but DRAM uses alternating current.
    E. Most people think SRAM tastes better than DRAM.
11. What, aside from capacity, is a significant difference between the MIPS register file and memories such as SRAM and DRAM?
    A. The MIPS register file can perform two read operations and one write operation in a single clock cycle, but SRAM and DRAM can perform just one read or one write operation at a time.
    B. The MIPS register file can perform two read operations and one write operation in a single clock cycle, but SRAM and DRAM can perform just one read and one write operation at a time.
    C. The MIPS register file can perform two read operations and one write operation in a single clock cycle, but SRAM and DRAM can perform just one read and two write operations at a time.
    D. There is no difference: they are the same thing.
    E. The register file uses a decoder to select which word will be written, but SRAM and DRAM do not use an address decoder: they just know automatically which word is to be read or written.
12. How many *address inputs* would a 64 GB byte-addressable memory have?
    A. 3
    B. 6
    C. 64
    D. 36
    E. 2^{36} (68,719,476,736)
13. Draw a diagram *here* that shows the sizes and names of the fields of an R-Format instruction:

14. Draw a diagram below that shows the sizes and names of the fields in an I-Format instruction:

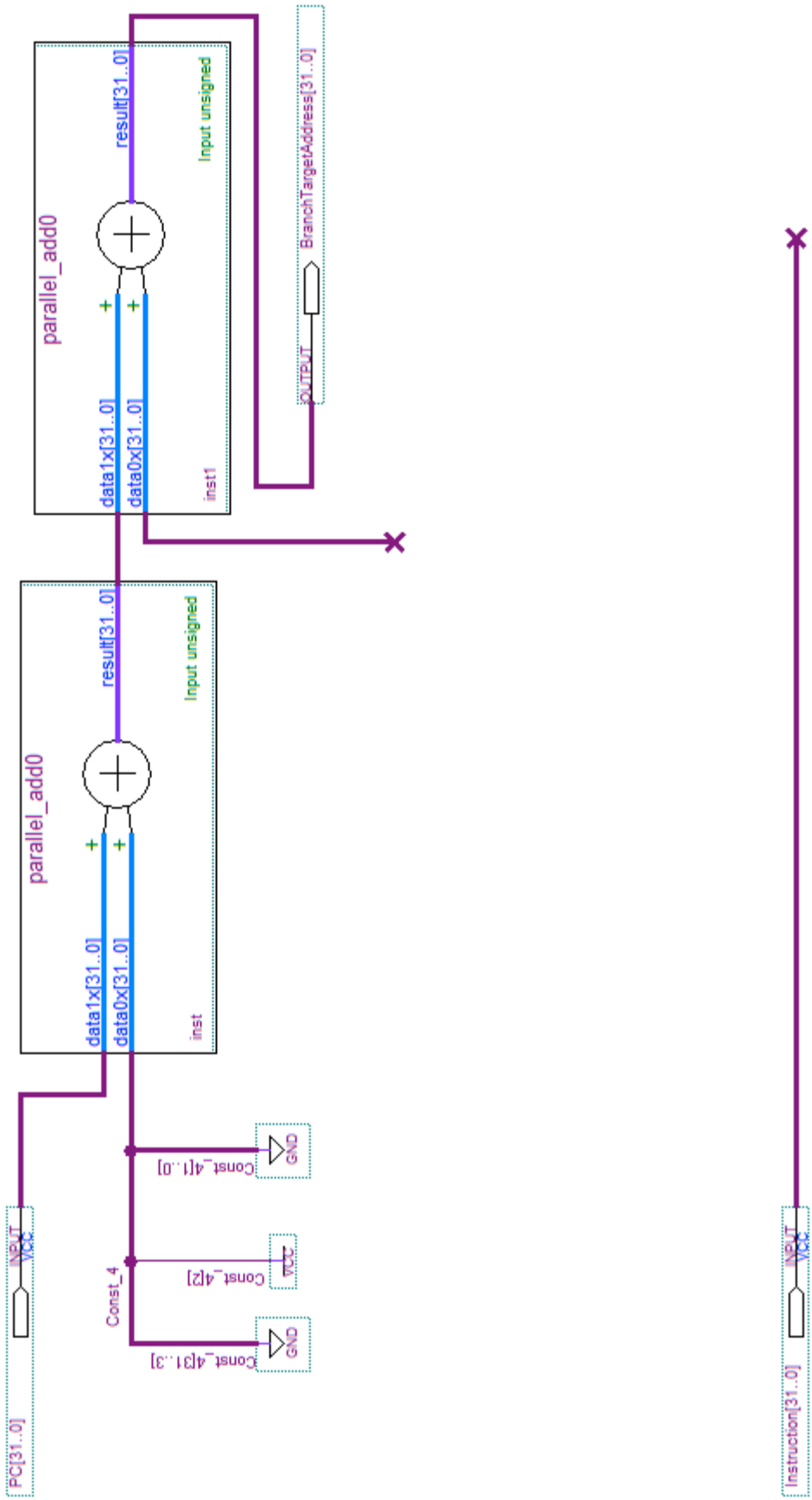
15. Draw a diagram below that shows the sizes and names of the fields in a J-Format instruction:

16. Give the *format name* (R, I, or J) for each of the following instructions:
    A. *beq* _____
    B. add _____
    C. andi _____
    D. lw _____
    E. j _____
17. Completely describe the execution of the *beq* instruction. You may use Verilog, pseudocode, English, or a mixture:

18. What *binary property* do all MIPS instruction addresses have in common, *and why*?

19. What would be a good name for the bus coming out of the l**eft** *parallel_add0* symbol in the diagram on the next page?

20. Complete the diagram on the next page so that it computes the Branch Target Address from the inputs and logic symbols already provided.


parallel_add0
result[31..0]
Input unsigned
data1x[31..0]
data0x[31..0]
inst1
BranchTargetAddress[31..0]
OUTPUT
parallel_add0
result[31..0]
Input unsigned
data1x[31..0]
data0x[31..0]
inst
Const_4
Const_4[1..0]
Const_4[2]
Const_4[31..3]
GND
VCC
GND
INPUT
VCC
PC[31..0]
INPUT
VCC
Instruction[31..0]